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Fabrication of Copper and Iron Nano/Micro Structures on Semiconducting Substrate and Their Electrical Characterization

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Abstract:
In this paper, we have studied the electrical properties of the randomly distributed metallic (Co and Fe) nano/micro wires on Silicon substrate. Deposition was carried out potentiostatically into the pores of the track-etch polycarbonate membrane spin coated onto the Si substrate. Spin coated films were irradiated with 150MeV Ni (+11) ions at a fluence of 8E7 ions/cm^2, followed by UV irradiation and chemically etching in aqueous NaOH (6N, at room temperature). The size, shape and morphology of the synthesized nano/micro structures is strongly dependent on the preparation conditions such as deposition potential, current density, electrolyte and etching conditions. Later, morphological and electrical properties of the so deposited nano-/micro structures were studied.
Keywords: *Irradiation, Ion track, etching.*

1. INTRODUCTION

In the recent years, there has been tremendous interest exhibited towards nano and micro pores in polymers generated by swift heavy ions due to vast variety of applications [1,2]. The technological importance of track-etched membranes is very significant due to their various applications particularly in the field of nano-/micro structural synthesis and their further use as devices in electronics. The pores are created by controlled chemical etching of the latent track created by irradiation of the polymeric film. The highly selective etching of tracks in polycarbonate makes it possible to produce membranes with pore diameters down to 10 nm [3]. By varying the ion fluence and the etching conditions, pores of different sizes and geometries are possible. This template technique enables the fabrication of wires with various shapes, in particular, conical or cylindrical.

The research on nano-/micro structures has led to the exploration of novel physics and material properties at reduced physical dimensions. There is considerable technological interest in the fabrication of arrays of high aspect ratio structures synthesized by electrodeposition for use as sensors and ultra-high-density information storage. Along with the synthesis of bare nano/micro structures, fabrication of one-dimensional nanostructures, or nanowires on the substrate (metallic or semiconducting), has been under intense investigation due to their lucrative device applications [4-6].

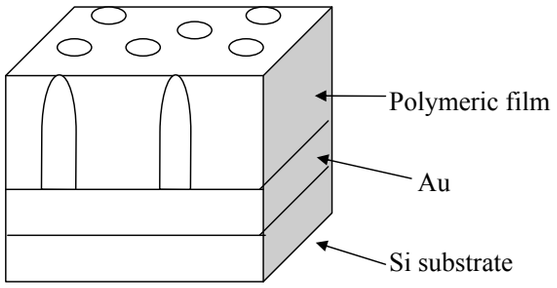

Figure 1: *Systematic picture of the template used for deposition.*

In the present work, the track-etched membrane is used to synthesis nano-/micro structures on the substrate itself. Structures are grown directly over the semiconducting substrate for their further characterization and obviating the need for post- synthesis manipulations. These Semiconductor based nano-/micro structures are expected to have practical applications in electronic circuit integration [7,8]. A thin polymeric layer was spin coated on the gold-coated semiconducting substrate. This gold layer acts as electrode at the time of electrodeposition and polymeric layer acts as template having the etched tracks.

2. EXPERIMENTAL DETAILS

Preparation of substrate was carried out at Inter University Accelerator Center (IUAC), New Delhi, India, and the CSIO, Chandigarh, India. We have used Si (P-doped) (111) as a semiconducting substrate. To remove the dirt and oxide layer from the surface of the substrate Si, wafer was kept in Trichloroethylene solvent at 70 ^{o}C for 10 min then immersed in 1% HF acid for 1 min. Finally wafer was rinsed using deionised water for 5 min.

A thin gold layer with thickness of about 95.5 nm was deposited using vacuum evaporation method, onto the Au layer, polycarbonate (Makrofol) was deposited by spin coating (at room temperature with spinning speed of 4000 rpm) and the thickness of coated polymer was around 10 μm. The adhesion of the polycarbonate film on the substrate was improved by the use of a primer (hexamethyledisilisazan), a chemical reagent $(CH_3)_3Si\text{-}NH\text{-}Si(CH_3)_3$, consisting of ammonia substituted with two trimethylsilyl functional groups.

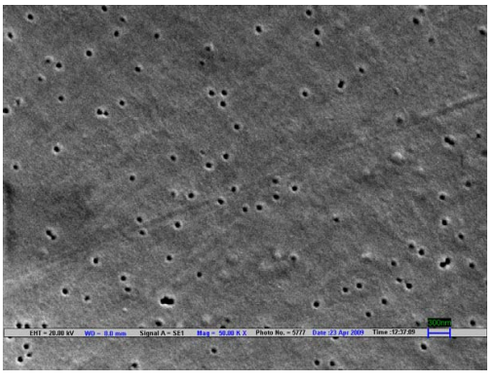

Figure 2(a): *SEM image of the etched pores on PC coated semiconducting substrate irradiated with Ni (150) MeV ions*

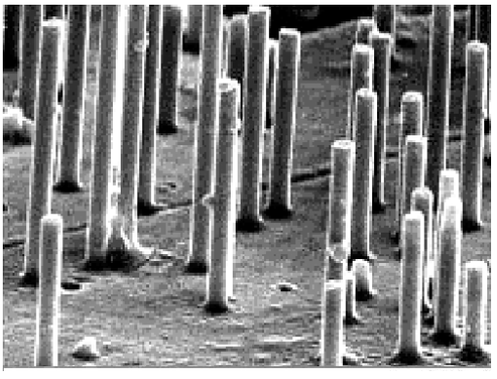

Figure 2(b): *SEM image of the electrodeposited copper nano/micro wires on the Si substrate.*

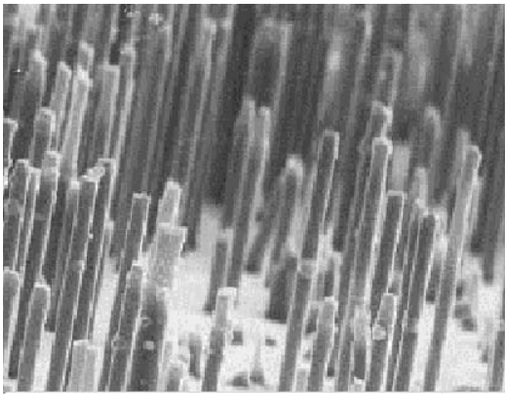

Figure 2(c): *SEM image of the electrodeposited iron nano/micro wires on the Si substrate*

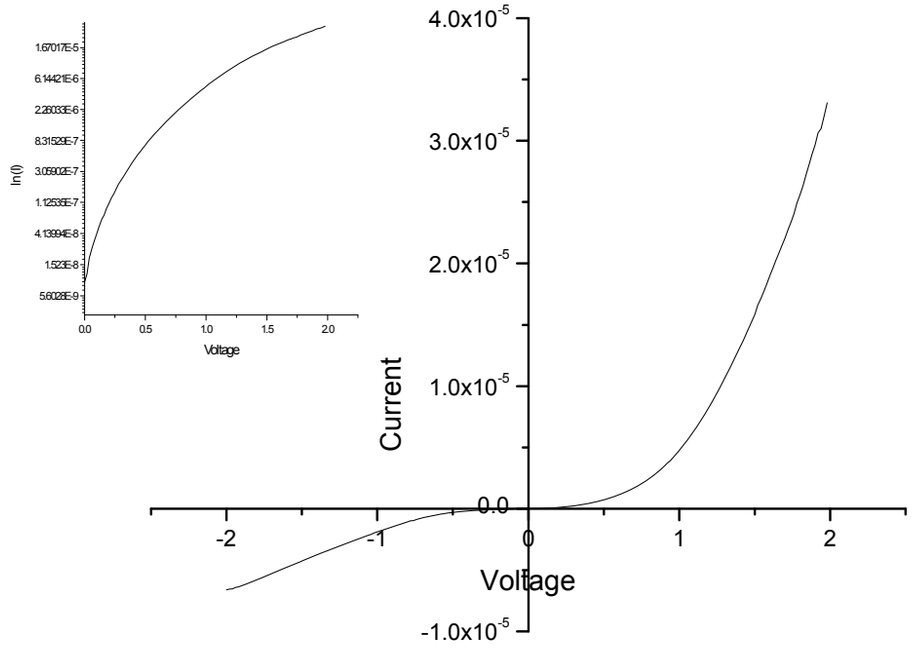

Figure 3 (a): *I-V characteristics of embedded copper nano/micro wires on Si substrate. Inset shows the variation of ln(I) with voltage(V).*

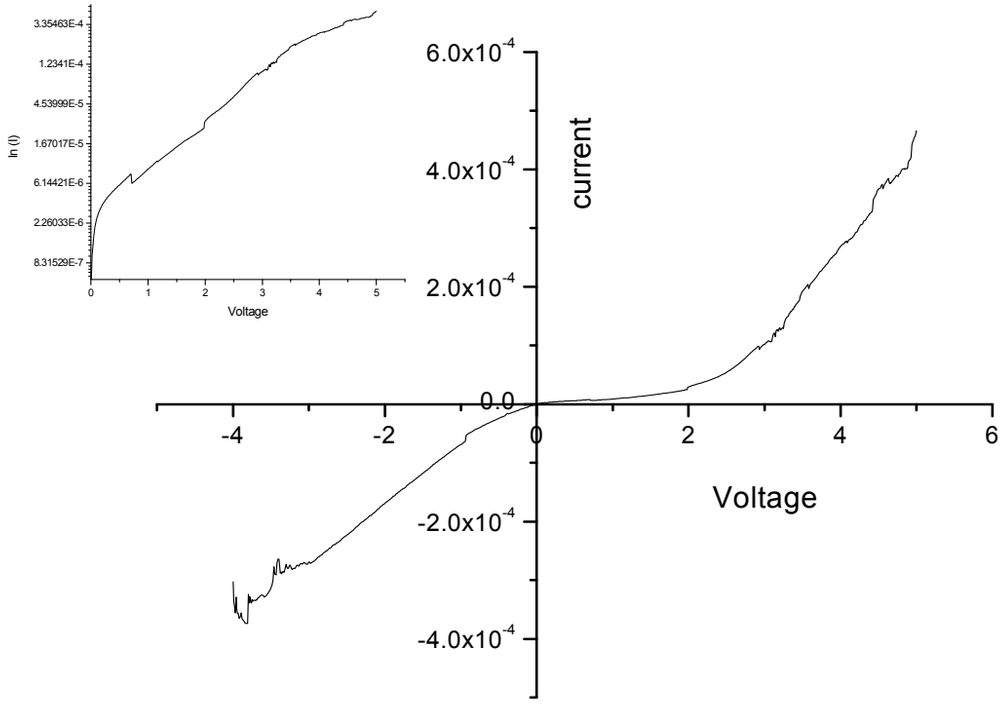

Figure 3(b): *I-V characteristics of embedded iron nano/micro wires on Si substrate. Inset shows the variation of ln(I) with voltage(V).*

The prepared samples were irradiated at room temperature with 150 MeV Ni^{+11} ions at a fluence of 8E7 at IUAC, New Delhi, India. Later, the irradiated samples were UV treated (365 nm, 150 W/cm^2) to increase the selectivity of the chemical etching thus favoring the formation of cylindrically shaped pores. Etching was performed in a home made one-compartment cell with a 6N NaOH aqueous solution at room temperature for a time up to 50 min.

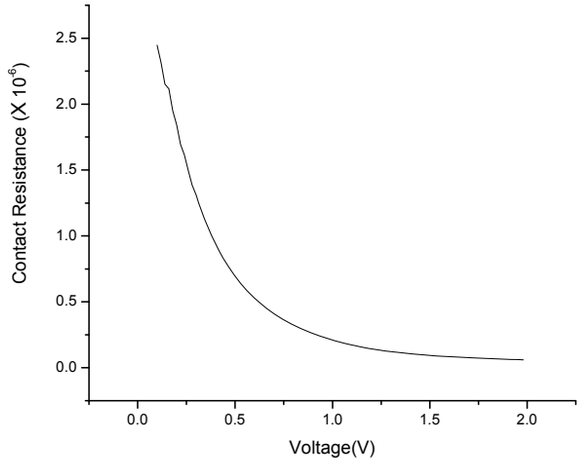

Figure 4: *The variation of resistance with applied bias for the Copper nano/ microwires on Silicon substrate*

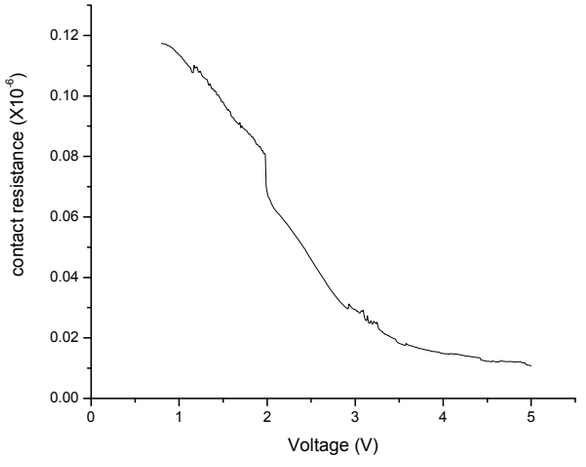

Figure 5: *The variation of resistance with applied bias for the Iron nano/ microwires on Silicon substrate*

The supported films were then immersed in an acetic acid solution and rinsed with milli-Q water at room temperature for 5 min and were then dried with hot air. It must be noted that the pore size depends both on the conditions of the ionic and UV irradiation, and on the conditions during chemical treatment of the tracks like nature and concentration of the reactants, temperature during etching, time duration for etching.

UV exposure leads to photo-oxidation in the polycarbonate and is able to increase the track etch ratio by an order of magnitude [9].

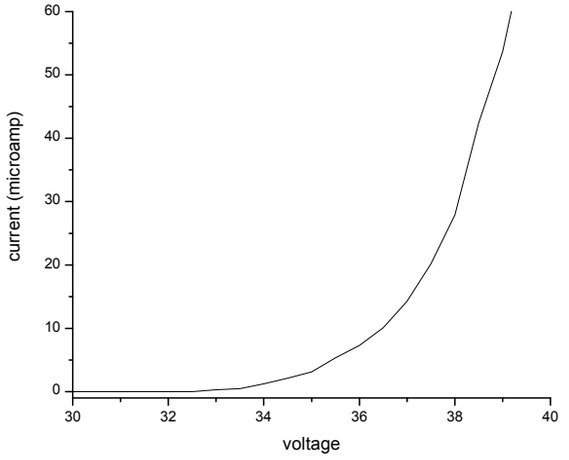

Figure 6 (a): *I-V curve of copper nano/micro wire on semiconducting substrate*

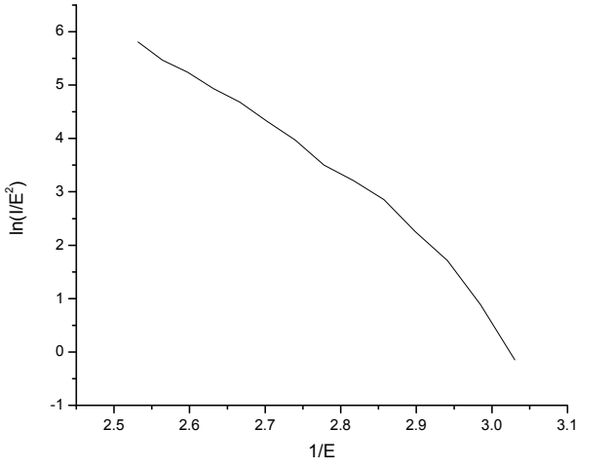

Figure 6 (b): *F-N plot of copper nano/micro wire on semiconducting substrate*

Electro-deposition within these pores of the supported template was performed at room temperature in a conventional one-compartment cell, with a copper rod working as anode and the gold layer as working electrode (cathode). An aqueous solution of $FeSO_4$ + H_2SO_4 and $CuSO_4$ + H_2SO_4 respectively, was used as electrolyte for the deposition of iron and copper into the pores.

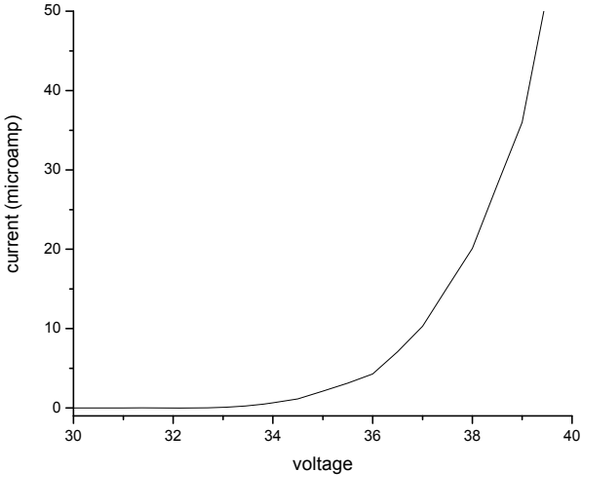

Figure 7 (a): *I-V curve of iron nano/micro wire on semiconducting substrate*

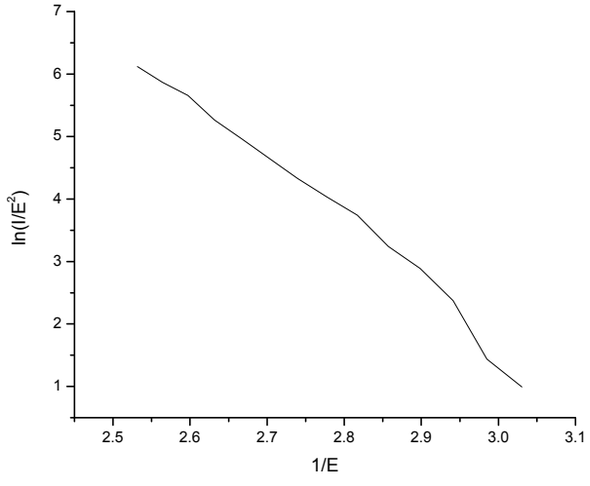

Figure 7 (b): *F-N plot of iron nano/micro wire on semiconducting substrate*

High concentration of electrolyte is important to provide a sufficiently large number of ions inside the pores during the galvanic deposition process. Nano-/micro structures were grown potentiostatically at 0.4 V. The deposition potential was applied using a power supply (Electromek INDIA, SAM- Model MR 85, 15 V) and the current and potential drop across the cell was monitored by digital multimeter (PHILIPS Digital Multimeter 1225).

After the deposition, substrate with nano-/micro wires was immediately removed from the electrolyte and then rinsed with double-distilled water and ethanol. Finally, it was dried in dry air at room temperature and subjected to further analysis. The porous thin polycarbonate membrane was removed by dissolving it in dichloromethane for 10 minutes and washed several times with double-distilled water.

3. RESULTS AND DISCUSSION

Using track -etched membrane technique, new templates consisting porous PC films supported on semi-conductive substrates have been prepared. Typical supported nanoporous template surface is shown in Figure 1.

In the present study, we have carried out morphological and electrical studies of template synthesized nano-/micro structures. For morphological characterization, the fabricated nano-/micro structures were viewed under SEM at SEMCF IIT New Delhi, Figure 2(a-c) shows the SEM images of pores so formed and Copper and Iron nano/micro wires grown on the silicon substrate.

The *in- situ* I-V characteristics of nano-/micro structures was carried out at room temperature by leaving the structures embedded in the insulating template membrane itself. A KEITHLEY 2400 source meter was used for the measurement. The Figure 3(a,b) shows the voltage vs current characteristics for the nano-/micro structures on the Silicon, it's the collective behavior of nanowires lying parallel to each other. Plot shows that at the metal- semiconductor contact system behaves non-ohmic when forward biased but in reverse biased region, variation is ohmic.

Under the forward biased V at a fixed temperature

$I = I_0[\exp\{(q(V-IR_s)/nkT)-1\}]$

n is the ideality factor and R_s is the diode series

resistance. For a pure thermionic emission n=1. Fit of linear region of the forward biased semi-log IV curve (where $V>3k_Bt$ and R_s is negligible) the value of ideality factor and Schottky barrier height can be determined. Extrapolation of straight line portion of the plot to V=0 gives I_0 and the slope S=d(lnI)/dV gives n.

Using I_0 barrier height may also be calculated using the equation

$$\Phi_B=(kT/q)(AA^*T^2/I_0)$$

Where A* is the Richardson constant and A is the electrical contact area [10].

Figure 3 (a,b) shows the variation of current with voltage for the nano/micro structures grown and inset give the semi-log plot for current and voltage. From these plots we can have the values of identity factor and saturation current for both the nano/micro structures grown on the silicon substrate. Table 1 gives the slope and intercept values for the same

Table 1

	Slope	Intercept
Copper	2.22	6.26E-7
Iron	1.24	2.88E-6

As the plots shows, the measured log I-V curve is not linear. Sze asserted that if thermionic emission is dominant, which is the major current flow mechanism for low impurity concentration, the curve should be linear [10]. Padovani and Stratton reported that even if thermionic-field emission is dominant, which occurs at a highly doped metal semiconductor interface, the log I-V curve is approximately linear [14].

While Lepselter and Andrews wrote that if direct tunneling is dominant, the current is directly proportional to applied bias [15,16], which implies that the contact is ohmic. However, our results in Figures 3 and 4 indicates that the contact do not follow any of the three models. Figures 4 and 5 shows the voltage dependence of the contact resistance. Contact resistance may be divided into two parts; the schottky diode resistance and spreading resistance caused by current crowding that is due to small size of contact. The nonlinear behavior depicted in Figure 3 and 4 is negligible for large size contacts. Schottky diode resistance depends on the applied voltage but spreading resistance depends on contact size and dopping level. So, as the applied voltage increases diode resistance approaches zero because of the increase in thermionic emission, and the net resistance measured gives spreading resistance. Therefore, from the results of Figure 4 and 5, we can deduce spreading resistance to be 0.0598E-6 Ω and 0.0107E-6 Ω for Copper and Iron, respectively.

According to Fowler-Nordheim theory [17], the field emission is described as tunneling through a potential barrier at the surface of solid when a large electric field is applied. Knowing some of the surface properties, one can calculate the probability of an energetic electron tunneling the potential barrier.

Considerable attention has been paid to the synthesis of various shaped nanostructures such as needles and tubules because of their unusual quantum characteristics as well as useful optical, electrical and field emission properties [18-21]. The electron field emission is one of the most interesting potential applications such as in cold cathode, miniature microwave generators, monochromatic electron sources and vacuum microelectronics [22-24]. Usually such applications require controlled growth of the nanostructures in size and shape in order to be capable of being used effectively as devices.

The oriented metallic array with bottom end on the semiconducting substrate was stuck on copper tape with the help of silver paste and was used as cathode. In this configureuration, arrays were placed with their long axes perpendicular to substrate and their tips acted as emitters. Field emission experiments were carried out in vacuum chamber with 2×10^{-5} Torr at room temperature of 29 ^oC. A copper plate with a diameter of 1 cm was used as anode. The average distance between the copper anode and a tip of silver arrays was 100 μm. The measured emission area was 100 mm^2. The emission current-voltage characteristics (Figures 6(a) and 7(a)) were analyzed by using the Fowler-Nordheim (FN) equation for the field emission [17].

$$J=A\,(\beta^2 V^2/\Phi d^2)\exp(-B\Phi^{3/2} d/\beta V),$$

Where J is the current density, A and B are constant, β is the field enhancement factor, Φ is the work

function, E=(V/d) is the applied field, d is the distance between the anode and the cathode and V is the applied voltage. The field enhancement factor β is calculated from the slope of the Fowler-Nordheim plot

The FN Plot (Figure 6(b) and 7(b)) almost followed a linear relationship confirming the electron-tunneling through the potential barrier.

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