Int. J. Nanosci. Nanotechnol., Vol. 15, No. 3, Sept. 2019, pp. 211-217

Short Communication

A Novel Design of Quaternary Inverter Gate Based on GNRFET

Mahdieh Nayeri[1], Peiman Keshavarzian[1,*] and Maryam Nayeri[2]

[1]Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran.
[2]Department of Electrical Engineering, Yazd Branch, Islamic Azad University, Yazd, Iran.

(*) Corresponding author: keshavarzian@iauk.ac.ir
(Received: 04 May 2018 and Accepted: 30 June 2019)

Abstract

This paper presents a novel design of quaternary logic gates using graphene nanoribbon field effect transistors (GNRFETs). GNRFETs are the alternative devices for digital circuit design due to their superior carrier-transport properties and potential for large-scale processing. In addition, Multiple-valued logic (MVL) is a promising alternative to the conventional binary logic design. Saving power and reduced chip area is the reason for simplicity. The first design is a resistive-load GNRFET-based quaternary inverter gate. The channel length is 15 nm. This circuit works with a 0.9V supply voltage at room temperature. For optimizing the first design, resistors are replaced with transistors in the second design. Simulation results using HSPICE indicate that in the second proposed design provides 61.1% reduction in power-delay product (PDP) that of first proposed. These results can be used in MVL design based on nano devices.

Keywords: *GNRFET, Inverter, Multiple-valued design, Power-delay product (PDP), Quaternary.*

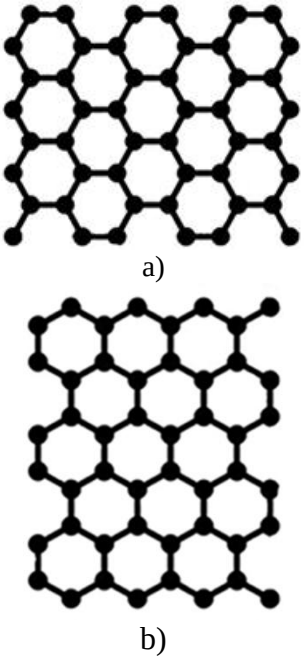
1. INRODUCTION

Various types of carbon allotropes are diamond, graphite, graphene, nanotubes, and fullerenes [1]. Graphene, a two-dimensional material with one atom thick structure, is ordered on a honeycomb lattice [2, 3]. Wonderful electronics properties of graphene [4] make it an alternate candidate for silicon in electronic devices such as field-effect transistors, tunnel barriers, and quantum dots [5, 6]. Planar geometry of graphene cause to process with more conventional complementary metal oxide semiconductor (CMOS) technology gives it a significant advantage over carbon nanotubes (CNTs) [7]. The major disadvantage of graphene is that it has lack of band gap [8]. Researchers offer three ways to open the band gaps of graphene: Using nanoribbon form of graphene, bilayer graphene and applying strain to graphene [9]. Graphene nanoribbon can open the bandgap up to 400 meV [10]. In this paper, we use graphene nanoribbon FETs to design the circuit. Armchair-edge (AGNRs) and zigzag-edge (ZGNRs) are the two types of graphene nanoribbon [11] as illustrated in figure 1. AGNRs are known to be the semiconductor and their electrical properties dependents on the ribbon width, whereas ZGNRs exhibit metallic and magnetic behavior. Thus, AGNR has been used for the digital circuits [12]. Single-layer graphene lattice consists of regular hexagons with a carbon atom at each corner. The width of a GNR (W_{ch}) is defined as follows [13]:

$$W_{ch} = (N-1)\sqrt{3}\frac{dcc}{2} \quad (1)$$

Where N represents the number of dimer lines as shown in figure 2(a). N is the number of dimer lines in the armchair

orientation and dcc= 0.144 nm is the carbon-carbon bond length. The electronic properties of armchair nanoribbon vary depending on the number of atoms on the edge. AGNR of type N = 3P+1 and N=3P are semiconductors whereas AGNR of type N=3P+2 is metallic where P is positive integer [14].



a)

b)

Figure1. *GNR-edge a) armchair edge, b) Zigzag edge.*

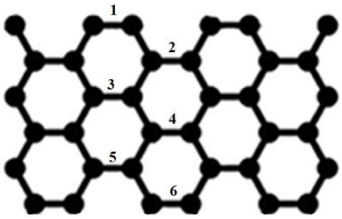


Figure2. *The Lattice structure of an armchair GNR with N=6.*

Graphene nanoribbon has the bandgap that depends on the nanoribbon width [15]. The SPICE compatible circuit model of GNRFETs [16] has been used for the circuit simulations. GNRFET could be a promising device for designing voltage-mode multiple-valued logic (MVL) circuits. In the multiple-valued logic more than two logic levels are defined depending on the number of levels, ternary (level=3) or quaternary (level= 4) logic styles [17]. The Complex process could be performed faster and fewer computation steps. MVL designs reduce the complexity of large chips and solve the challenge facing the CMOS technology. Many complex applications such as estimation, analysis procedures decision systems and process control are not possible in the binary logic. In addition, the whole power dissipation can be reduced by translating a design from the binary to the ternary or quaternary families [18-21]. Raychowdhury *et al.* [22] designed a ternary logic gate by using CNTFET and resistors. Lin *et al.* [23] have eliminated the resistors by applying active CNTFETs. A dynamic structure for implementing a dynamic ternary logic based on the complete model technique was proposed in [20]. Moaiyeri *et al.* [24] have designed quaternary maximum (QMax) and minimum circuits (QMin) based on CNTFETs. They found that their designs provide very high robustness to the effect of process variations. The quaternary full adders based on CNTFETs have designed by Moaiyeri *et al.* [25]. They showed that this proposed design reduces considerably average power, and static power consumption. Kim *et al.* [26] have realized experimentally n-type ternary graphene field effect transistors (TGFET) and p-type TGFET to illustrate ternary inverter circuit. Their findings show three discrete current states in one device at room temperature. The multiple-valued logic circuits can be implemented by one [24] or more than one power supply voltages [28]. Therefore, increase in the number of power supply sources would lead to complexity in interconnections, less energy consumption, and higher fabrication cost. We use one power supply source for multiple-valued logic circuits [29]. Hence, the voltage division rule is applied to produce different voltages for different logic values.

In the remainder of this paper, in section 2 MVL is reviewed in more detail. The new design method and circuits are presented and described in section 3. The

Section 4 includes the simulation results and finally, section 5 concludes the paper.

2. PROPOSED DESIGNS

The important parameter for designing the MVL circuit is threshold voltage (V_{th}). The band gap energy is proportional to the threshold voltage and inversely proportional to the width of graphene nanoribbon. Therefore, different widths of GNR have the different threshold voltage. Quarternary logic includes four logic levels which can be illustrated by 0,1,2 and 3 symbols. These logic levels contain 0V,1/3 Vdd, 2/3 Vdd and Vdd voltage levels, respectively [30]. The truth table of quaternary inverter gate is given in Table 1 [31, 32].

Table 1*.Truth table of quaternary inverter*.

Input	*Symbol*	*Out put*
0	0	*Vdd*
1/3 *Vdd*	1	2/3 *Vdd*
2/3 *Vdd*	2	1/3 *Vdd*
Vdd	3	0

The parameters of the GNRFET model [33], their values, and brief descriptions are given in Table 2.

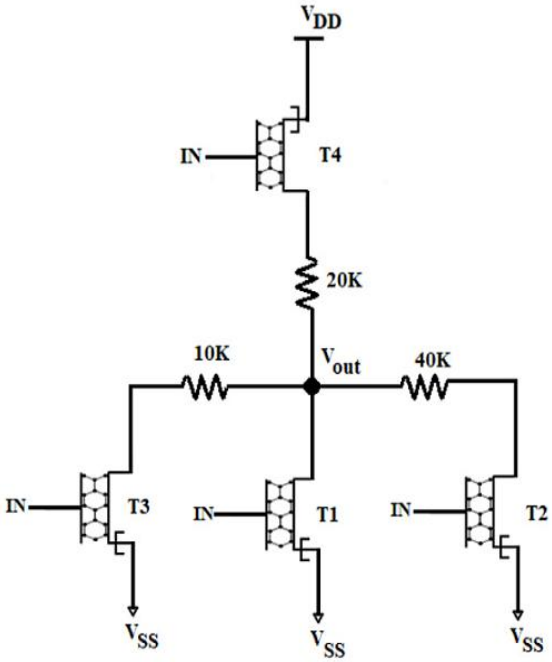
2.1. The First Proposed Design

The proposed inverter gate consists of three resistors and three GNRFET, is shown in figure 3(a). The power supply voltage is 0.9V. The threshold voltages of n-type GNRFETs are 0.9V, 0.3V, 0.6V respectively.

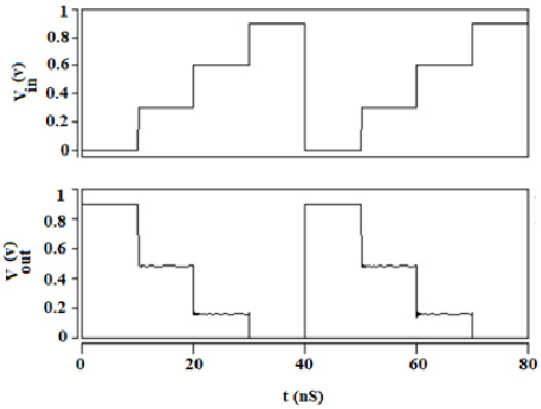
As seen in figure 3(a), when the input value is 0V, all n-type GNRFETs are off and only p-type GNRFET (T4) is on. Therefore, the output is *Vdd*. When the input value reaches around 1/3 *Vdd*, only T4 and T2 are on and the output is 2/3 *Vdd*. By increasing the input value to 2/3 *Vdd*, T4, and T3 are turned on and the output becomes 1/3 *Vdd*. Finally, if the input value is *Vdd*, all of the n-type GNRFETs are on and the output is 0V. The transient responses of the proposed design are demonstrated in figure 3b.

Table2*.The important HSPICE parameters of the GNRFET*

Device parameter	Description	Default value
L	Physical channel length	15nm
Tox	The thickness of top gate dielectric material (planer gate)	0.95nm
2Wsp	The spacing between the edges of two adjacent GNRs within the same device	2 nm
NRib	The number of GNRs in the device	6
P	The edge roughness percentage of the device	0
Dop	Source and drain reservoirs doping fraction	0.001
Tox2	Oxide thickness between channel and substrate/bottom gate	20nm
Gates_tied	Whether Gate or sub hold the same voltage	0



a)



b)

Figure 3*. a) The First proposed design. b) The transient response.*

2.2. The Second Proposed Design

In the second design, for quaternary inverter gate, we replace resistors with transistors because it leads taking less chip area. Delay significantly is reduced by using transistors.

In similar HSPICE parameters with the first design, results show that PDP of the second proposed design is 2609.34×10^{-21} and the PDP of the first one is 4268.16×10^{-21}. The second design achieves more than 160% improvement over in terms of PDP.

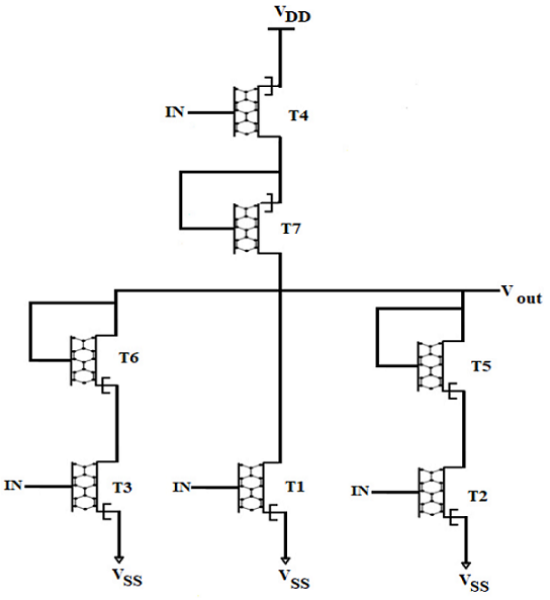


Figure 4*.The Second proposed design.*

3. Simulation Results and Discussion

The power, delay and product delay-power are the figure of merit for GNRFET. Therefore, we obtain these parameters with the different number of ribbon (nrib). As depicted in figure 5, delay increases by increasing the nrib. This variation is high in first proposed design while the variation is low in second proposed design.

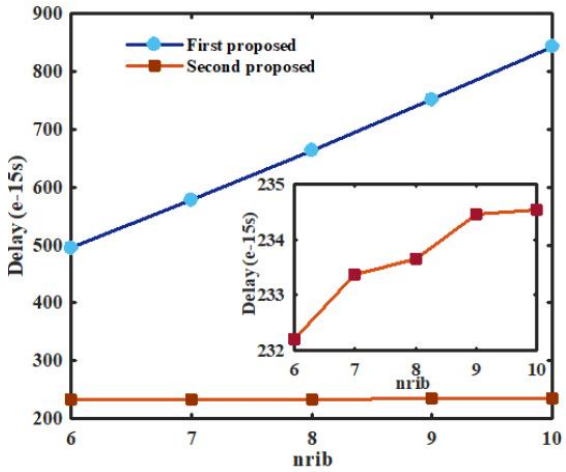


Figure.5. *Maximum delay versus nrib, inset: zooming in a portion of delay-nrib curve.*

In addition, by increasing the nrib, power increases. According to figure 6, increasing the power is more obvious for second proposed design than first proposed design.

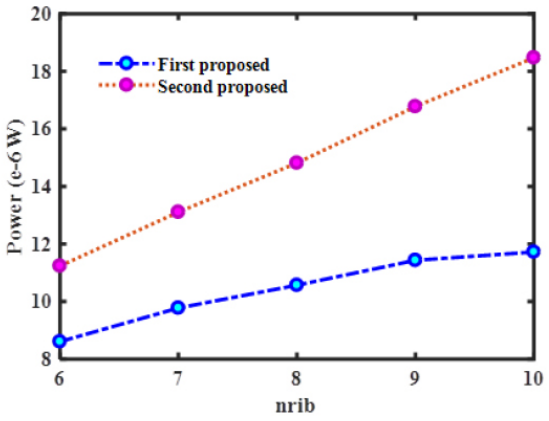


Figure 6*.Power as a function of nrib.*

As seen in figure7, the second proposed design has the less PDP than the first proposed design. In the first design, PDP increases significantly by increasing nrib whereas PDP slightly increases in the second design. Thereby, second proposed design can be a suitable design for

quaternary inverter gate based on GNRFET.

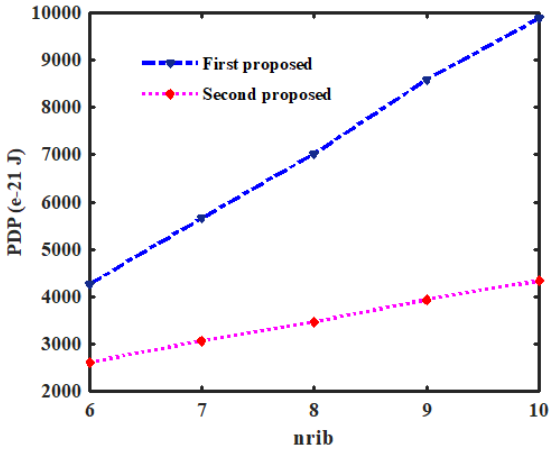


Figure 7*.PDP versus nrib.*

Fabrication technology of GNRs cannot produce perfectly smooth edges. The misfit edges result in a phenomenon called edge roughness, which affects the properties of GNRs. Edge roughness reduces Ion. Therefore, the delay increases. Edge roughness leads to a little decrease in power consumption. As shown in Figure 8, PDP escalates with increasing of edge roughness percent.

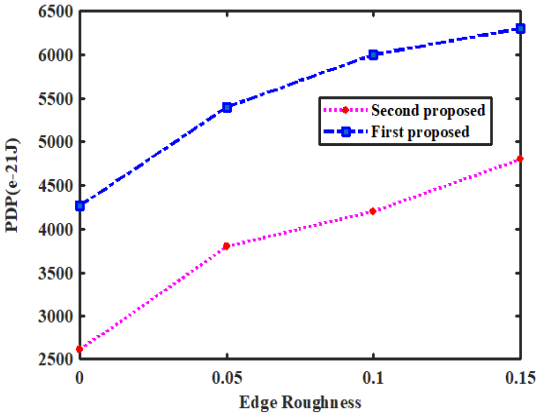


Figure 8*.PDP versus edge roughness.*

The variation of oxide thickness (Tox) as a function of PDP has investigated in figure 9. I on decreases as Tox increases and delay increases. Power is reduced when Tox is increased. As a result, PDP has decreases, which is shown in figure 9.

The results show that PDP for our proposed circuits is significantly improved. These studies promise attractive future opportunities for researchers in this field.

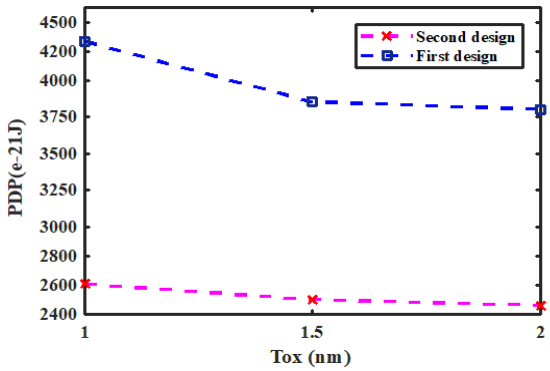


Figure 9*.PDP versus Tox*

Table 3 compares our proposed circuits based on GNRFET with quaternary inverters based on CNTFET in Ref [30, 31].

Table3. *Performance comparison of the quaternary Inverter*

Proposed design	Max Delay (ps)	Avg Power(uw)	PDP (aJ)
First design	0.5	8.5	4.2
Second design	0.22	11.8	2.59
Design of [34]	102.68	1.69	173.52
Design of [35]	487.37	1.247	607.750

4. CONCLUSION

In this paper, we designed a quaternary inverter gate based on GNRFET for the first time. The first circuit design has consisted of three transistors and three resistors. In the second design, resistors have replaced with transistors because of large-area that resistor occupied. The second design has six transistors. Delay has reduced significantly than the first design. However, power is increased in the second design. Overall, PDP is decreased in second design remarkably. Then, we investigated the effect of increasing the number of ribbon in GNRFET. By increasing the number of ribbons, power, delay, and PDP is increased. This variation of first design is more sensible than second design. This circuit can be utilized for other circuit based on GNRFET such as the full adder, comparator, and decoder and so on.

REFERENCES

1. Gogotsi, Y., (2015). "Not just graphene: The wonderful world of carbon and related nanomaterials", *MRS Bulletin*, 40: 1110-1121.
2. Ghozatloo, A., Yazdani, A., Shariaty-Niassar, M., (2017). "Morphology Change and Structural Evaluation of Carbon Nanostructures", *International Journal of Nanoscience and Nanotechnology*, 13: 97-104.
3. Bhimanapati, G. R., Lin, Z., Meunier, V., Jung, Y., Cha, J., Das, S., ..., Liang, L., (2015). "Recent advances in two-dimensional materials beyond graphene", *Acs Nano*, 9: 11509-11539.
4. Utkan, G., Ozturk, T., Duygulu, O., Tahtasakal, E., Denizci, A.A., (2019). "Microbial Reduction of Graphene Oxide by Lactobacillus Plantarum", *International Journal of Nanoscience and Nanotechnology*, 15: 127-136.
5. Vicarelli, L., Heerema, S. J., Dekker, C., Zandbergen, H. W., (2015). "Controlling defects in graphene for optimizing the electrical properties of graphene nanodevices", *ACS nano*, 9: 3428-3435.
6. Reddy, D., Register, L. F., Carpenter, G. D., Banerjee, S. K., (2011). "Graphene field-effect transistors", *Journal of Physics D: Applied Physics*, 44: 313001.
7. Gholipour, M., Masoumi, N., (2014). "Graphene nanoribbon crossbar architecture for low power and dense circuit implementations", *Microelectronics Journal*, 45: 1533-1541.
8. Farazas, A., Mavropoulos, A., Christofilos, D., Tsiaousis, I., Tsipas, D., (2018). "Ultrasound Assisted Green Synthesis and Characterization of Graphene Oxide", *International Journal of Nanoscience and Nanotechnology*, 14: 11-17.
9. Rabieefar, F., Dideban, D., (2019). "Utilizing Graphene Nano-Ribbon Transistor in Data Converters: A Comparative Study", *ECS Journal of Solid State Science and Technology*, 8: M30-M37.
10. Akbar, F., Kolahdouz, M., Larimian, S., Radfar, B., Radamson, H. H., (2015). "Graphene synthesis, characterization and its applications in nanophotonics, nanoelectronics, and nanosensing", *Journal of Materials Science: Materials in Electronics*, 26: 4347-4379.
11. Nayeri, M., Keshavarzian, P., Nayeri, M., (2019). "High-Speed Penternary Inverter Gate Using GNRFET", *Journal of Advances in Computer Research*, 10: 1-9
12. Celis, A., Nair, M. N., Taleb-Ibrahimi, A., Conrad, E. H., Berger, C., De Heer, W. A., Tejeda, A., (2016). "Graphene nanoribbons: fabrication, properties and devices", *Journal of Physics D: Applied Physics*, 49: 143001.
13. Choudhury, M. R., Yoon, Y., Guo, J, Mohanram, K., (2011). "Graphene nanoribbon FETs: Technology exploration for performance and reliability", *IEEE transactions on nanotechnology*, 10: 727-736.
14. Chen, Y. Y., Sangai, A., Rogachev, A., Gholipour, M., Iannaccone, G., Fiori, G., Chen, D., (2015). "A SPICE-compatible model of MOS- type graphene nano-ribbon field-effect transistors enabling gate-and circuit-level delay and power analysis under process variation", *IEEE Transactions on Nanotechnology*, 14: 1068-1082.
15. Marmolejo-Tejada, J. M., Velasco-Medina, J., (2016). "Review on graphene nanoribbon devices for logic applications", *Microelectronics Journal*, 48: 18-38.
16. Hur, J. H., Kim, D. K., (2018). "Theoretical investigation of performance of armchair graphene nano ribbon field effect transistors", *Nanotechnology*, 29: 185202.
17. Sharifi, F., Moaiyeri, M.H., Navi, K., Bagherzadeh, N., (2015). "Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach", *Microelectronics Journal*, 46: 1333-1342.
18. Bajec, I. L., Zimic, N., Mraz, M., (2006). "The ternary quantum-dot cell and ternary logic", *Nanotechnology*, 17: 1937.
19. Raghavan, B. S., Bhaaskaran, V. K., (2017). "Design of novel Multiple Valued Logic (MVL) circuits", In *Nextgen Electronic Technologies: Silicon to Software (ICNETS2), International Conference on* (. 371-378). IEEE.
20. Sahoo, S. K., Akhilesh, G., Sahoo, R., Muglikar, M., (2017). "High-Performance Ternary Adder Using CNTFET", *IEEE Transactions on Nanotechnology*, 16: 368-374.
21. Moaiyeri, M. H., Mirzaee, R. F., Doostaregan, A., Navi, K., Hashemipour, O., (2013). "A universal method for designing low-power carbon nanotube FET-based multiple-valued logic circuits", *IET Computers & Digital Techniques*, 7: 167-181.
22. Raychowdhury, A., Roy, K., (2005). "Carbon-nanotube-based voltage-mode multiple-valued logic design", *IEEE Transactions on Nanotechnology*, 4: 168-179.
23. Lin, S., Kim, Y. B., Lombardi, F., (2011). "CNTFET-based design of ternary logic gates and arithmetic circuits", *IEEE transactions on nanotechnology*, 10: 217-225.
24. Moaiyeri, M. H., Rahi, A., Sharifi, F., Navi, K., (2017). "Design and evaluation of energy-efficient carbon nanotube FET-based quaternary minimum and maximum circuits", *Journal of applied research and technology*, 15: 233-241.

25. Moaiyeri, M. H., Sedighiani, S., Sharifi, F., Navi, K., (2016). "Design and analysis of carbon nanotube FET based quaternary full adders", *Frontiers of Information Technology & Electronic Engineering*, 17: 1056-1066.
26. Kim, Y. J., Kim, S. Y., Noh, J., Shim, C. H., Jung, U., Lee, S. K., ... Lee, B. H., (2016). "Demonstration of complementary ternary graphene field-effect transistors", *Scientific reports*, *6*, 39353.
27. Mahani, A. T., Keshavarzian, P., (2017). "A novel energy-efficient and high speed full adder using CNTFET", *Microelectronics Journal*, 61: 79-88.
28. Sharifi, F., Moaiyeri, M. H., Navi, K., Bagherzadeh, N., (2016). "Ultra-low-power carbon nanotube FET-based quaternary logic gates", *International Journal of Electronics*, 103: 1524-1537.
29. Ebrahimi, S. A., Reshadinezhad, M. R., Bohlooli, A., Shahsavari, M., (2016). "Efficient CNTFET-based design of quaternary logic gates and arithmetic circuits", *Microelectronics Journal*, 53: 156-166.
30. Sharifi, F., Moaiyeri, M. H., Navi, K., Bagherzadeh, N., (2015). "Quaternary full adder cells based on carbon nanotube FETs", *Journal of Computational Electronics*, 14: 762-772.
31. Keshavarzian, P., Navi, K., (2009). "Universal ternary logic circuit design through carbon nanotube technology", *International Journal of Nanotechnology*, 6: 942-953.
32. Sharifi, F., Moaiyeri, M. H., Navi, K., Bagherzadeh, N., (2016). "Ultra-low-power carbon nanotube FET-based quaternary logic gates", *International Journal of Electronics*, 103: 1524-1537.
33. Illinois University GNRFET model website. Illinois University, Available: http://dchen.ece.illinois.edu/tools.html
34. Doostaregan, A., Abrishamifar, A., (2019). "A New Method for Design of CNFET-Based Quaternary Circuits", *Circuits, Systems, and Signal Processing*, 38: 2588-2606.
35. Liang, J., Chen, L., Han, J., Lombardi, F., (2014). "Design and evaluation of multiple valued logic gates using pseudo N-type carbon nanotube FETs", *IEEE Transactions on Nanotechnology*, 13: 695-708.