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CNTFET-Based Analog and Digital Circuits: Design, Simulation and Comparative Analysis

Roberto Marani[1] and Anna Gina Perri[2*]

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Abstract

In this paper, a procedure, that allows a comparative analysis of A/D circuits implemented in CNTFET and MOS technologies, is proposed. As an example of analog circuit, the design of a basic current mirror is considered, while, as an example of digital circuits, a NAND gate is considered. All simulations are performed using the Verilog-A programming language.

Keywords: CNTFET, CMOS, modeling, analog and digital (A/D) circuits, Verilog-A

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1. Introduction

CNTFETs are Field Effect Transistors having a Carbon NanoTube as a channel [1-22].

In this paper, a comparative analysis of A/D circuits implemented in CNTFET and MOS technologies is proposed.

For the first technology, the CNTFET model, proposed in [2-3], is used while for the second one the BSIM4 model of the Advanced Design System (ADS) library, written in Verilog-A [23], is used.

As an example of analog circuit, the design of a basic current mirror is examined, while, as an example of digital circuits, the design of a NAND gate is considered.

2. CNTFET and MOSFET models used

An exhaustive description of the used CNTFET model is in [2-3]. Therefore, the reader is encouraged to consult these references, where the following expression of the total drain current is explained [24]:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

The C-V model used is fully described in [2-3] and therefore the reader is encouraged to consult these references:

$$\begin{cases} C_{GD} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{Dp}}\frac{\partial V_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{Sp}}\frac{\partial V_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

The equivalent circuit of an n-type CNTFET is shown in Figure 1.

For the MOSFET model, the BSIM4 model of the ADS library is used [25].

3. Experimental Setup and Methodology

3.1 Basic Current Mirror Design in CNTFET and MOSFET Technology

The basic current mirror consists of two active components as shown in Figure 2, where a current sink is based on n-type C-CNTFET.

The reference current I_{REF} of 10 μA is provided by an ideal current supply on the left branch of the circuit. This current sets the quiescent point of M1 in the saturation region and provides bias voltage at the gate of M2, which must faithfully follow the I_{REF} as long as output voltage $V_{DD} \geq V_T$, the voltage required to switch M2 on.

The drain voltage of M2 is swept in order to evaluate how well the output current replicates an ideal current supply. The output current value is given by [26-27]:

$$I_{out} = k'\left(V_G - V_T\right)^2\left(1+\lambda V_{DD}\right) \quad (3)$$

The same was done using NMOS devices.

The I_{OUT} values are shown in Figure 3, where a

[1] *Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy.*

[2] *Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, Italy.*

E-mail: annagina.perri@poliba.it

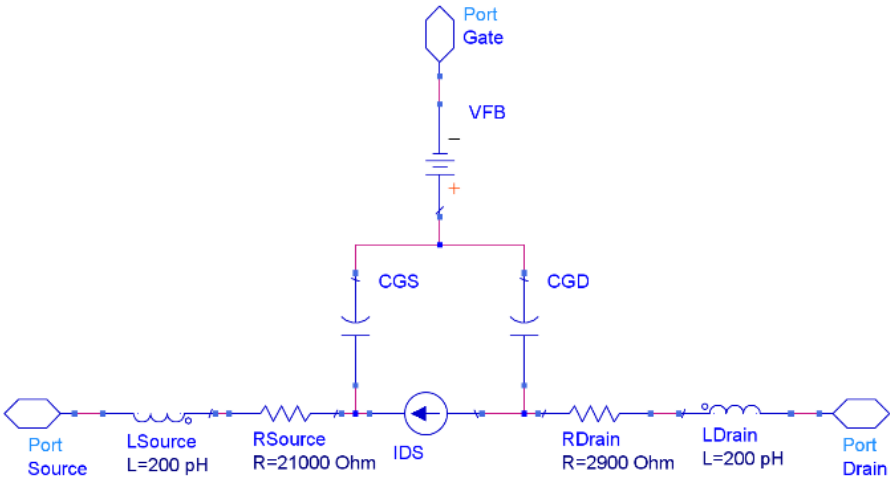

Fig. 1. Equivalent circuit of an n-type CNTFET.

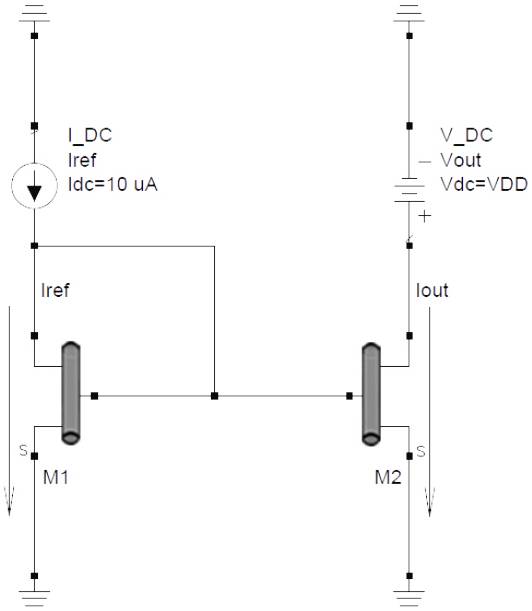

Fig. 2. Basic current mirror circuit with an n-type CNTFET.

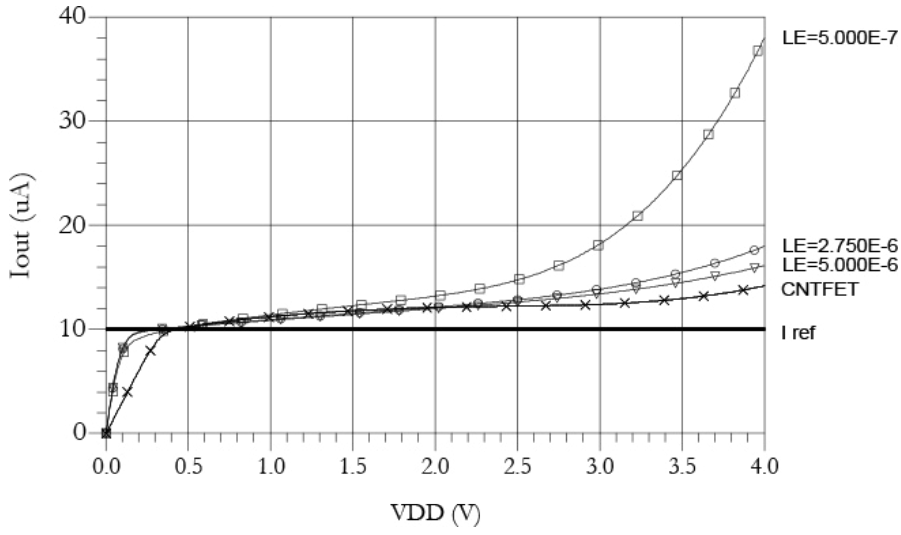

Fig. 3. Reference current versus VDD in an n-type basic current mirror.

comparison with MOSFETs having different channel length L and constant aspect ratio, W/L = 2, is illustrated.

The simulation underlines that n-type CNTFET works better than MOSFETs of a larger size, as validated in Figure 4, where the error in current replication given by $|I_{OUT}-I_{REF}|$ is shown.

In Figures 5 and 6 other simulation results are reported.

The Figures 5 and 6 indicate that the NMOS current mirrors provide better performances in terms of current replication error, for lower values of W/L.

3.2 CNTFET and MOSFET NAND Gate Design

The circuit used to design and characterize a NAND gate for CNTFET technology is shown in Figure 7.

For this circuit, a single voltage supply, denoted as V_{DD}, has been used.

By sweeping Vgs from 0 to V_{DD}, the simulated Voltage Transfer Characteristics (VTC), at different values of supply voltage, are reported in Figures 8 and 9.

These Figures indicate that for voltage supply smaller than 0.1 V, the regenerative characteristic is worse than at 0.5 V.

Figure 10 allows for the evaluation of the NAND propagation delay, equal to $1.1^{x}10^{-12}$ s.

In CMOS technology, the best obtained results for VTC is shown in Figure 11, while Figure 12 shows the CMOS NAND propagation delay ($1.8^{x}10^{-10}$ s).

1 provides a comparison with the results obtained for a NOT gate, in order to demonstrate that the proposed procedure may be applied to characterize and design any logic gate [28-29].

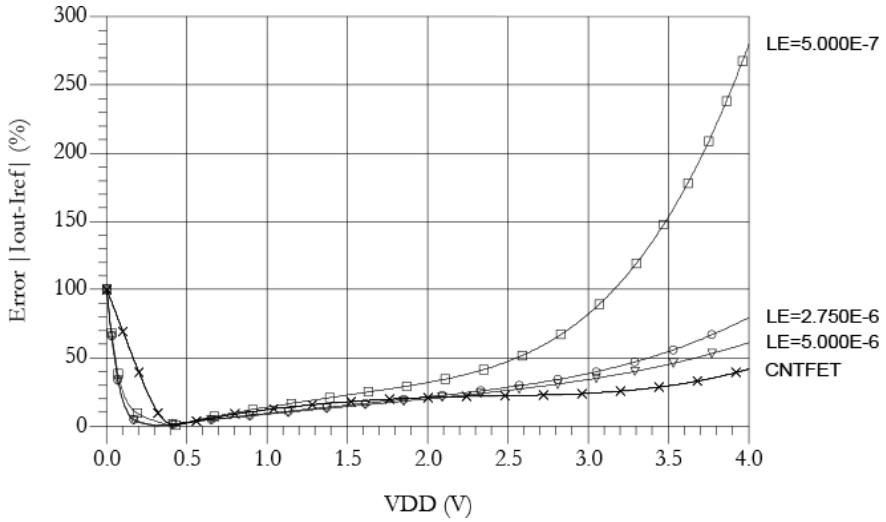

Fig. 4. Relative error $|I_{OUT}-I_{REF}|$ in current replication of an n-type basic current mirror.

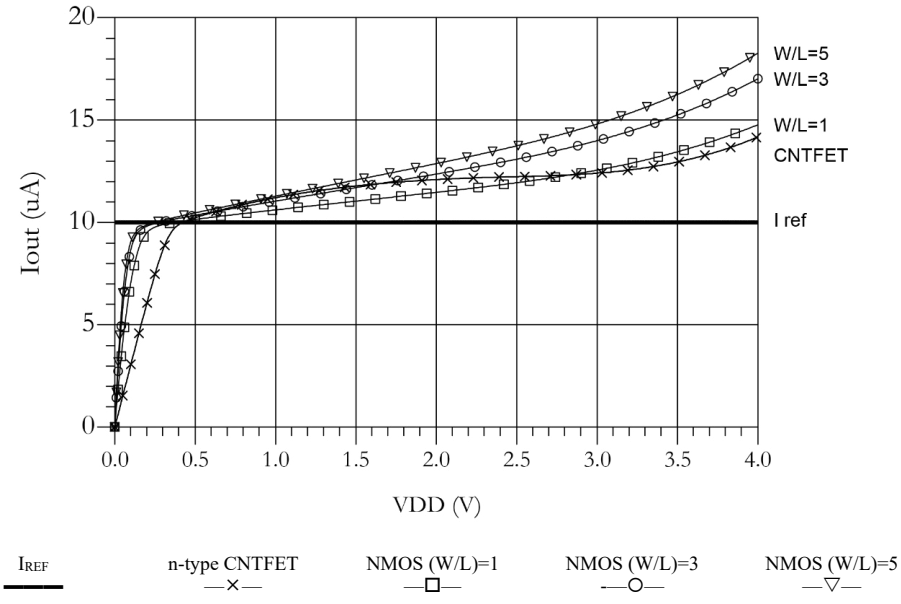

Fig. 5. IOUT versus VDD in an n-type basic current mirror for different W/L values.

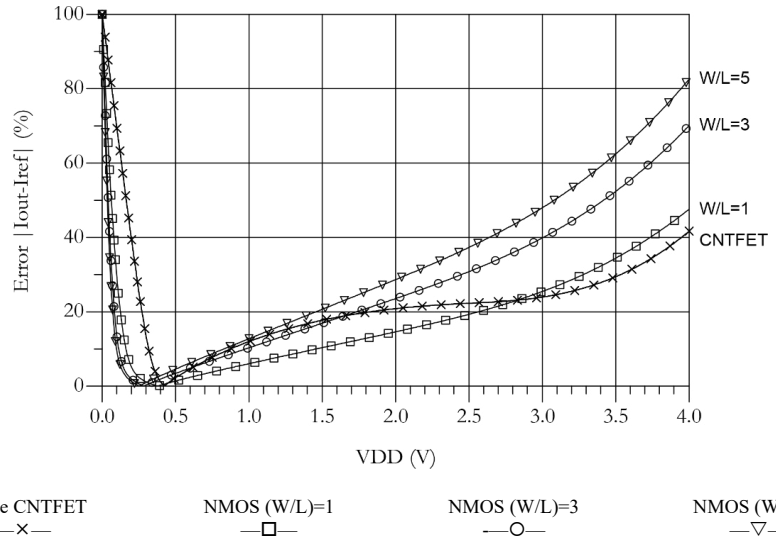

Fig. 6. Relative error $|I_{OUT}-I_{REF}|$ versus V_{DD} in an n-type basic current mirror for different W/L values.

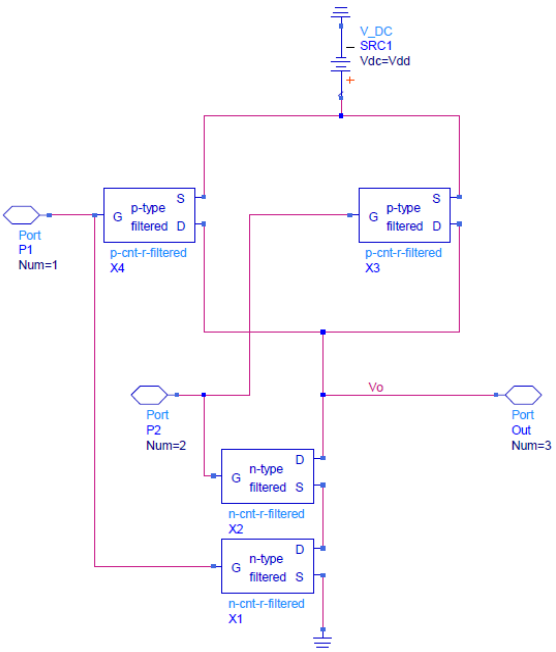

Fig. 7. CNTFET NAND gate.

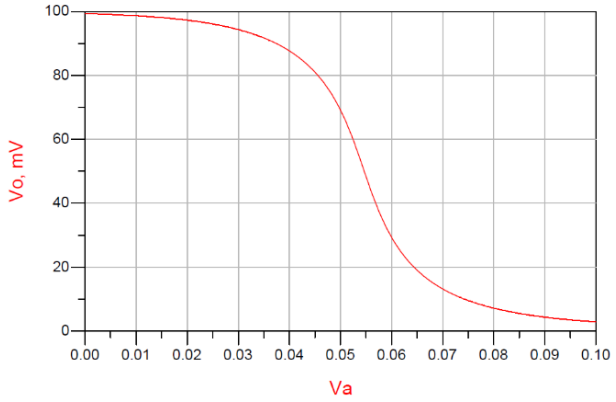

Fig. 9. VTC at VDD = 0.1 V.

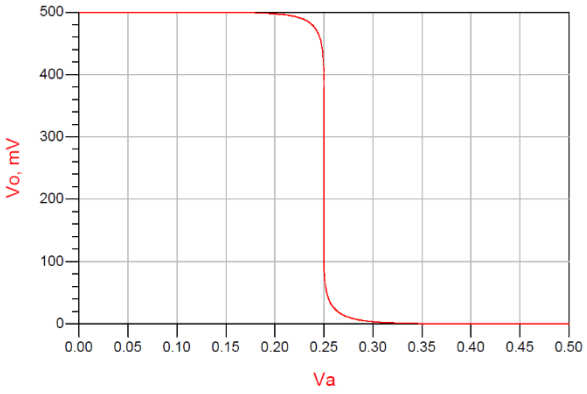

Fig. 8. VTC at VDD = 0.5 V.

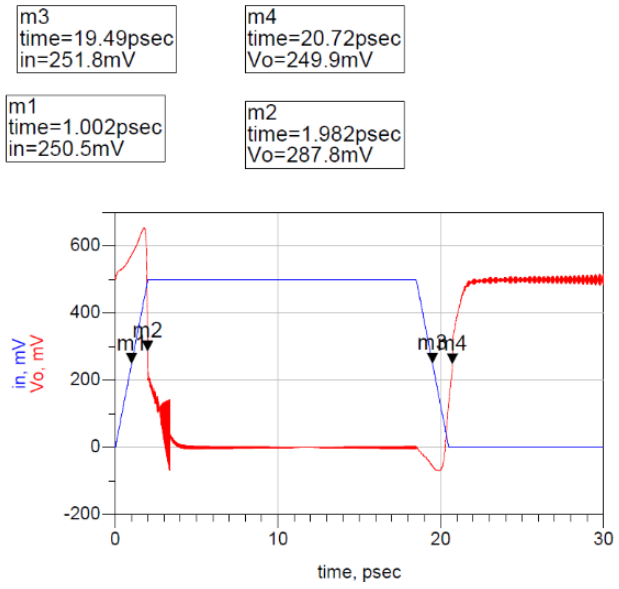

Fig. 10. NAND gate propagation delay

Table 1. Summary of simulation results.

Technology	CNTFET	CMOS
PDF (J)	$3.32^{x}10^{-18}$	$5.80^{x}10^{-13}$
Frequency (Hz)	$50^{x}10^{9}$	$200^{x}10^{6}$
τ_P (s)	$1.52^{x}10^{-12}$	$2.50^{x}10^{-10}$
V_{DD} (V)	0.5	3

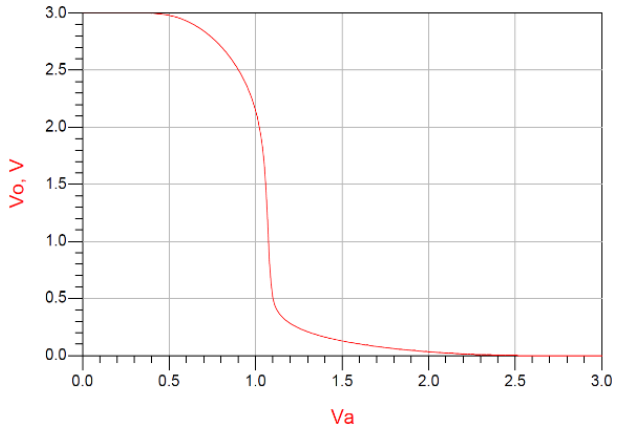

Fig. 11. VTC at VDD = 3 V.

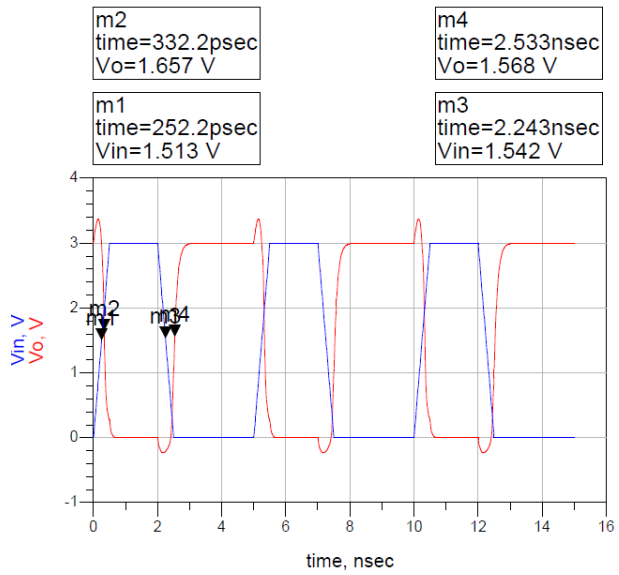

Fig. 12. CMOS NAND gate propagation delay

4. Conclusions and Future Developments

A procedure, that allows a comparative analysis of A/D circuits in CNTFET and MOS technologies, has been proposed.

To make further comparisons, the proposed technique will be repeated considering other CNTFET models [30-31].

Moreover, the effects of noise [32-34] and the impact of CNTFET technology [35-36] will be analyzed more thoroughly.

Conflict of interest

The authors declare that they have no conflict of interest.

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