Int. J. Nanosci. Nanotechnol., Vol. 18, No. 3, Sept. 2022, pp. 197-208

Low Power Soft-Error Hardened Latch Implemented by Carbon Nanotube Field-Effect Transistors

Mahnaz Soltani Mohammadi[1,*], Sirus Sadughi[2] and Farhad Razaghian[1]

[1]Department of Electrical Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran
[2]Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran

(*) Corresponding author: sadughi@sharif.edu
(*Received: 27 October 2021 and Accepted: 12 April 2022*)

Abstract

A soft error hardened latch is designed, which is based on carbon nanotube field-effect transistors (CNTFETs). The nanoscale circuits are more susceptible to transient or soft errors due to reduced stored charge in their sensitive nodes. Hence, an energy efficient design is a significant challenge, particularly for storage elements like latches. The proposed hardened latch consists of a Schmitt trigger circuit to mask the transient errors, a memory cell, and a C-element with an inverter at its output. The delay element followed by a C-element and a memory cell structure filters single event transient (SET) effectively and has improved robustness against single event upset (SEU). CNTFETs are substituted to gain all the benefits of nanotubes, such as robustness, temperature stability, high speed, and low power consumption. The implementation results in 32nm technology indicate a power consumption of 11.33nW for the supply voltage of 0.9V. The designed latch has low power consumption and lower power-delay product (PDP) concerning the design in CMOS technology. Compared to reported CNTFET latches, the simulation results indicate that, in addition to lower area requirement the proposed latch is more resistant to energetic particles strike than other similar latches and the rise and fall time of the proposed structure is between 12 to 15 ps in different conditions.

Keywords: *Hardened latch, Carbon nanotube FET, Schmitt trigger, C-element, soft error, Memory cell.*

1. INRODUCTION

From the viewpoint of reliability, systems can be divided into critical and non-critical systems in practical applications. It is evident that reliability is one of the outmost necessities; nevertheless, the advanced technology requires that even in non-critical applications, reliability be considered an important issue. The reason is that the occurrence of multiple faults indicates the unreliability of the product, which also risks the market of future products. Therefore, reliability for all applications, including critical and non-critical, is an important parameter [1, 2].

Failures in circuits based on nanometer technologies can be divided into permanent failure and transient failure. Permanent failure disables the system permanently with improper performance. However, transient failures occur due to environmental changes, and their effects are temporary. The transient failure caused by high-energy particles of cosmic rays or by alpha particles penetrating the sensitive regions of semiconductor chips is of significant importance because of their distribution density and energy. When a high-energy particle strikes the sensitive region of a semiconductor chip, a dense channel of electron and hole is formed. The presence of an electric field causes the movement of these charge carriers in the circuit, and if they can charge or discharge a capacitor in the hit node, a transient voltage pulse will be generated [3].

Meanwhile, the content of a memory element may be affected, and its logic may change, in which case a soft error has occurred. In a desirable environment, about 90 percent of the faults in a computer system are transient faults. Therefore, transient failures are of greater importance in evaluating the error rates and system crash rates [3].

In recent trends in scaling down the channel length of transistors, the short channel effects have become more serious. Moreover, scaling down transistor feature size creates challenging problems such as high power density and high leakage currents, which are critical, particularly in VLSI systems that are battery-powered or energy-limited powered [4, 5]. On the other hand, in circuits with novel devices in nanoscale, since the nodes' capacitors and the supply voltage are smaller, the amount of charge on the nodes is smaller. Lower charge on sensitive nodes of the circuit is a serious problem, and these circuits are susceptible to voltage variations caused by alpha particles and cosmic ray neutrons [6, 7]. Also, the process variations in the new technologies have become more critical. Cosmic particles can pass through the silicon substrate and generate minority carriers collected by the drain and source that can change the node voltages, resulting in transient fault. This fault is critical in information storage cells like memories and latches because of information change, called soft error [8, 9].

As the particles strike the logic gates and pass through the logic circuits, the injected charge generates a transient voltage wave at the output called single event transient (SET). If the high-energy particles simultaneously affect multiple nodes of a digital circuit's hybrid section, then it is called multiple event transient (MET).

The transient voltage waves caused by striking high-energy particles during transmission and propagation can be masked out by logic or electronic structure to prevent further transmission and propagation in the latch's sampling period. These remedies reduce the probability of soft error occurrence to some extent, but many transient waves with adequate time latency reach the storage elements. Such transients result in fault and soft error if they pass through ordinary coatings and reach sequential sections during the sampling period and, consequently, store as data. The strike of particles directly affects the internal nodes of the memory circuit and changes the circuit states. This phenomenon is known as a single event upset (SEU). If multiple nodes of the sequential section are affected by the strike of high-energy particles, it is called the multiple events upset (MEU) [10, 11].

The strike of particles on control circuitry such as clock pulse circuits might be the false triggering of control signals, which can generate unwanted information storage and timing violations [12].

To evaluate the tolerance capability of latches against transient faults caused by high-energy particles, simulations are performed using a model introduced in [13, 14], which is a double exponential model. In this model, the current curve I(t) is given by the following equation:

$$I(t) = \frac{Q}{\tau_1 - \tau_2}\left[\exp\left(-\frac{t}{\tau_1}\right) - \exp\left(-\frac{t}{\tau_2}\right)\right] \quad (1)$$

Q_{crit} is the charge injected into the striking region, τ_1 and τ_2 are time constants. They are known as the collection time constant and the time constant for the initial establishment of the ion track, respectively. This current model is used to calculate Q_{crit} in latch circuits. The area under the current curve I(t) represents the amount of charge created in the particle affected node. If the charge exceeds Q_{crit}, an unexpected glitch might appear in the output voltage waveform. A node with a higher Q_{crit} is more tolerant of soft error. The amount of Q_{crit} is estimated for sensitive nodes with less charge accumulation to model the soft error. After the specification of the circuit's sensitive nodes, the current pulse model of particle charge accumulation is utilized for those

nodes [15]. Figure 1 shows soft error modeling for a CMOS inverter. Parts (a) and (b) represent high to low and low to high transient faults caused by discharging and charging current spikes.

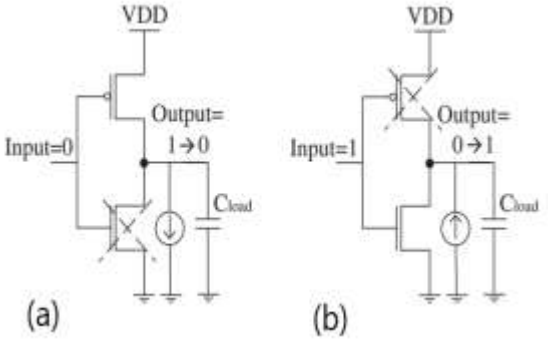

Figure 1. *Soft error modeling (a) high to low transient faults (b) low to high transient faults [16].*

Various methods have been proposed to reduce the soft error caused by SEU. Error correction codes (ECCs) and methods for designing hardened memory cells and sequential elements are presented in [17]. The simplest form of hardening technique for the logic structure to mitigate soft errors is the increase of stored node charge and proper gate sizing to prevent transient wave propagation as much as possible. But employing this method reduces circuit speed and increases power consumption, moving against the technology trend [18]. Considering the present technology, half of the faults are caused by storage elements [19]. Thus, memories, flip-flops, and latches have also received special attention for making them more hardened to soft errors [20-22]. Studies show that logic circuits have become more sensitive to soft errors [23, 24]. A study of energy distribution and neutron spectrum indicates that the density of low-energy particles is higher than the density of high-energy ones [25]. Thus, as the circuit dimensions decrease, the critical charge decreases. The circuit is affected by lower energy particles with higher density; hence, soft error probability increases. On the other hand, considering the present technology with the growing density of circuit components, the probability of multiple nodes of a circuit being affected by high-energy particles (MET soft error) has increased.

There have been various techniques to harden latch circuits against soft errors, described in the following. One technique for soft error hardening is the dual interlocked cell (DICE) based on spatial redundancy. This circuit structure is shown in Figure 2. It consists of p-device and n-device loops, one is clockwise, and the other is counterclockwise [26]. This circuit is accompanied by a standard 6T memory cell [27] and used in pulsed latch and flip flops [27, 28]. Although the hardened structures based on DICE can eliminate the effect of particle strike, they require increased power consumption, more area, and they are susceptible to input noise [28].

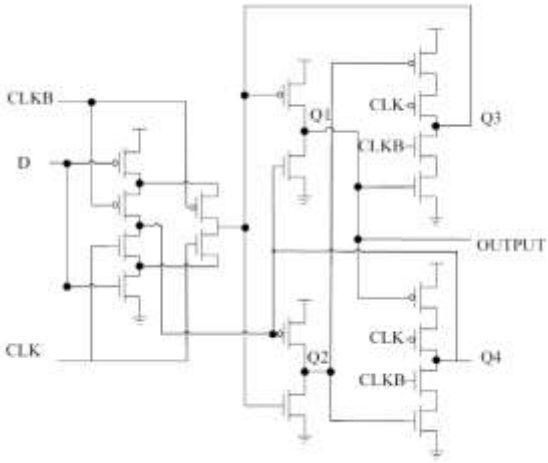

Figure 2. *DICE latch [26].*

In the spatial redundancy technique, multiple versions of data are processed simultaneously, and then the final value is selected by voting. One of these techniques is the triple modular redundancy (TMR) which converts the conventional latch to a TMR-latch. Triple module redundancy is one of the critical techniques for hardening, and it is widely used. In this technique, one version is repeated three times, and the voting circuit is inserted at the output to make the majority the circuit output. Although this technique effectively reduces the soft error rate, it always incurs

large area overhead and high power consumption (Figure 3) [29, 30].

The temporal redundancy technique is based on using multiple delayed versions of data and the main version. This technique can eliminate all noises which have a smaller time period than delay. Although this technique increases the total delay of the circuit, it is used more often than the previous technique due to incurring a smaller area and lower power consumption [30, 31].

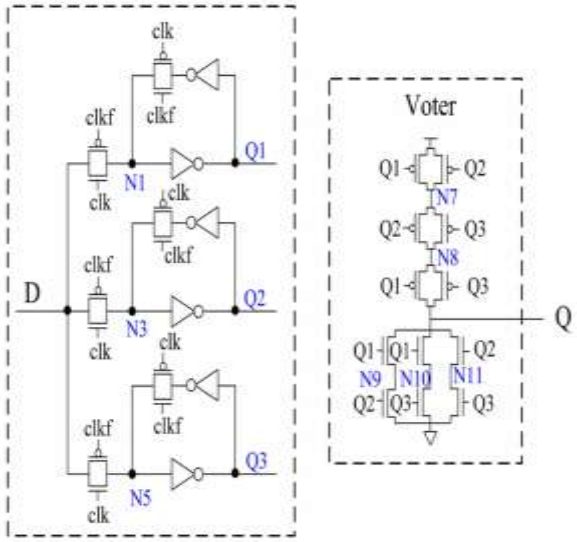

Figure 3. *TMR Latch [30].*

2. A BRIEF REVIEW OF CARBON NANO-TUBE FIELD EFFECT TRANSISTORS

As stated before, this paper's goal is to design a soft error hardened latch using carbon nanotube transistors. CNTs discovered by L.V. Radushkevich and V.M. Lukyanovich in 1952 and Iijima introduced CNTs to the world in 1991 [32]. These materials have unique thermal, mechanical, chemical, and physical properties because of their cylindrical structure, nanoscale, and high length to diameter ratio. Thus, CNTs construct devices like transistors, sensors, field-emission displays, and nanotube memories. One of the most applicable fields for CNTs is electronics. With the rapid development of integrated circuits, scientists look for new techniques in circuit implementations. Considering the higher performance, higher carrier velocity, higher transconductance, and lower power consumption, CNTFET demonstrates significantly better performance than the conventional CMOS transistors [33].

CNTs are rolled-up graphene sheets with sp^2 hybridization and hexagonal lattice categorized single-wall CNTs (SWCNT) and multiple-wall CNTs (MWCNT). SWCNT is a graphene sheet that is tubed as a cylinder. By tubing the graphene sheet as a cylinder such that the beginning and the end of the lattice vector align in the graphene sheet, a nanotube with lattice vector (n,m) is obtained. The lattice vector specifies the chirality of the nanotube. There are various chiralities, including nanotube with zigzag, armchair, and chiral vectors. The electric properties of the CNTs depend on their chirality. MWCNTs comprise concentric cylinders with a specific distance among their layers, where each tube might have a different chirality. The diameter of the CNTs varies from nanometer in SWCNTs to tens of nanometer in MWCNTs. Their length is usually about a few micrometers [34, 35].
CNTs are used in transistors due to their semiconductor property and in connections due to their conduction property. SWCNTs outperform MWCNTs in conductance, bandwidth, predictability (semiconductor or conductor), and controllability. Thus, they are used to construct transistors. Zigzag CNTs are used to construct transistors, and they are used as the channel between drain and source. An example of these transistors is shown in Figure 4.

The critical parameters of these transistors are the nanotube diameter and the threshold voltage, which are calculated using Eq. (2) and Eq. (3), respectively.

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + mn} \qquad (2)$$

$$V_{TH} = \frac{a(V_\pi)}{\sqrt{3}qD_{CNT}} \qquad (3)$$

In these equations, $a_0 = 0.142$ nm is the atomic distance between carbon atoms, and V_π is the bonding energy between carbon atoms, m and n also constitute the chiral vector. Here, since a zigzag nanotube is used, the chiral vector is (m,0) [36].

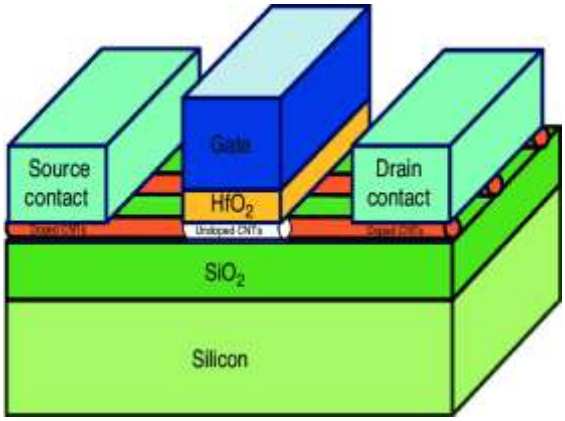

Figure 4. *Carbon nanotube field-effect transistor [36].*

3. THE PROPOSED CIRCUIT

CNTs like Graphene and another thin film is ideal alternatives to Silicon transistors due to their unique properties such as small dimensions, high speed, low power consumption, and performance similar to MOSFETs [40-43]. On the other hand, the high resistance and tolerance of CNTs considering their small dimensions compared to conventional semiconductors, make them suitable for hardware in commercial or space applications. CNT-based logic designs demonstrate an improved tolerance to SETs as compared to the MOSFET-based designs. In the following, a soft-error hardened latch is designed and simulated, which has improved performance. The proposed hardened latch was first designed in CMOS 180nm technology, and a post-layout simulation was performed. Level 3 was used to design PMOS transistors due to the mobility difference of PMOS and NMOS transistors. It was considered to use the minimum allowable size for the length and width of the transistors so that a smaller capacitance is generated between the nodes. Therefore, the size of the proposed circuit is smaller than the similar ones. Figure 5 shows the structure of the proposed hardened latch using CNTs. Figure 6 illustrated the layout schematic in the 180 nm technology of CMOS. The size of the proposed circuit is 3100 μm^2. The proposed hardened latch has a smaller area as compared to the similar reported works.

Several structures have been proposed for the latch circuit in various works, including the HPRL[a] structure and their application in circuits with the ability to interrupt the clock pulse. Since it is impossible to enter new data to the latch circuit, the relevant sub-circuits must be such that the node's logic in them due to the high impedance state and the leakage current not be lost. In other words, no node should be permanently in the high impedance state. Because the position of the nodes in this state, especially for today's technologies, due to high leakage currents, can lead to loss of its logic. The main problem of the HPRL circuit is that during the latch hold period and when the output node logic is changed by striking energetic particles until this logic is regenerated, other stages of circuits may have sampled this logic incorrectly and resulting in a soft error. But if the input of the next stages is also determined comparatively, for example, by the C-element, this problem will be solved. In the HPRL structure, due to the division of the input node and consequently having a similar node in terms of logic with the output node, a higher resistance of this node against the energetic particles strike is expected. The main problem in the LPRL[b] structure and VLPRL[c] was the sensitivity of the single output node to the energetic particle strike; because this node has no other copy and cannot be retrieved if its logic is changed. On the other hand, in the hold mode of the latch circuit, all middle nodes are fed from the output node, and as a result, by changing the logic of this node, all middle nodes are also

[a] High Performance Robust Latch
[b] Low Power Robust Latch
[c] Very Low Power Robust Latch

affected. The only way out of this mode is to enter new data to the latch [40-43].

However, in the structure called HPRL, the output node in the hold mode of the latch alone does not feed all the middle nodes. In other words, if the logic of this node changes due to the energetic particle strike, the middle nodes are temporarily in a high impedance state, and the output node logic is revived. The middle nodes are again out of the high impedance state by reviving the output node logic and returning to their normal state. In the proposed structure, the general nodes of the circuit are divided into three categories in terms of sensitivity to the energetic particles strike: In the first category, although the logic of the corresponding node changes with the particle strike, its effect is not seen in the output node. Single nodes and pairs of middle nodes are placed in this category. Hence, it affects the nodes at the same time and leads to a change in their logic. The third case will occur when it is affected by the cosmic ray, but the output node has not lost its logic.

In the second category, when the energetic particle strikes, the logic of the hit node changes, but after a period of time, the logic of that node is revived. For example, the output node is in this category, and the energetic atomic particle strike with this single node can be regenerated. In the third category, particle strike changes the output node logic and can only be recovered by restarting the system or arrival a new clock pulse and sampling new data. To check the circuit's performance, suppose the clock pulse signal is in the "0" mode. It should be logical, and the so-called latch should be in a transparent mode. Assuming the output node is in the "1" mode, it will be in the "1" mode due to the similarity of the output node's logic in the normal mode of the circuit operation due to applying the clock pulse signal counter wise to the middle sections. Now suppose the clock pulse signal changes mode, and then the latch enters the hold mode. In this case, the direct path from the input to the output is closed. In this case, the output changes mode, and the output node will be temporarily in high impedance state and will maintain its logic. After a limited time, hit nodes will return to their previous logic, and by reactivating the output stage, the output node will amplify its previous logic.

In the above-proposed structures, due to the identification of sensitive nodes, it is necessary to design at the layout level so that these nodes are physically spaced from each other so that the particle strike cannot affect all of them simultaneously. Therefore, the soft error probability caused by a single event transient (SET) and a single event upset (SEU) is greatly reduced. Because the HPRL structure is more robust than the other two structures, so in this section, only the physical layout of this structure is designed. In the case of a high-energy particle strike with the proposed physical layout, the physical distance of the sensitive nodes from each other simultaneously affects the probability of these nodes, and the resulting soft error is very low.

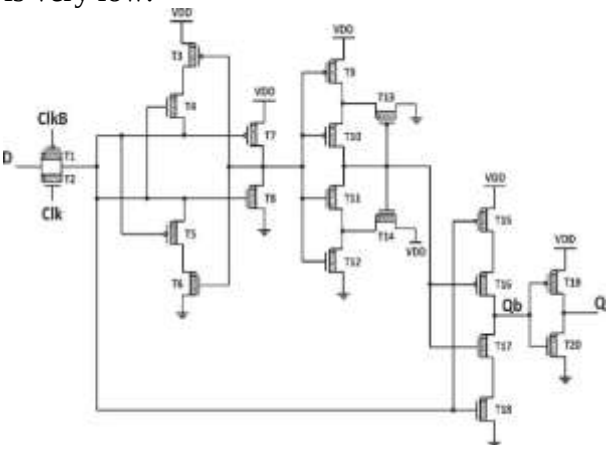

Figure 5. *Schematic of the proposed hardened latch using CNT.*

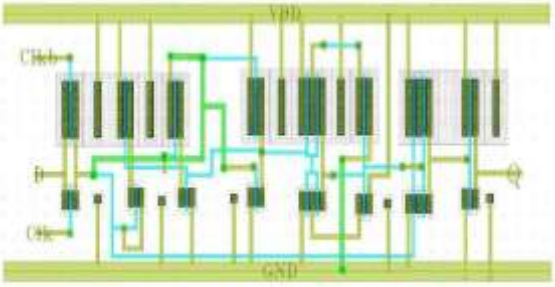

Figure 6. *Layout of the proposed hardened latch in 180nm CMOS technology.*

Schematic of the proposed hardened latch using CNTs and its layout are shown in Figure 5 and Figure 6, respectively. The proposed hardened latch consists of a set of transmission gates comprising transistors T_1 and T_2, a memory cell (transistors T3, T4, T5, T6, T7, T8), a Schmitt trigger in one of the forward paths, and a C-element with one inverter at the output. In this latch structure, D is the input, and Q is the output. Clk and clkB are the clock signal and the inverted clock signal, respectively. The proposed hardened latch structure with a delay element accompanied by a C-element for filtering the SET. A memory cell has improved tolerance against SEU and filters the SET.

The proposed latch consists of two forward paths from the input D to the output Q. A path is directly connected to one of the C-element inputs at the output. And the other forward-path consists of a memory cell and a Schmidt trigger connected to the other input of the C-element. Using this method, the SET pulse is masked. Since the Schmitt trigger circuit has high filtering capability due to symmetric structure, when the clk signal is "high," the latch is in transparent mode. The transmission gate comprising transistors T1 and T2 is on. And input D is transmitted to the output via two separate forward paths. The SET pulse in input is thus filtered. When the clk signal is "low," the transmission gate comprising transistors T1 and T2 is off. Therefore, the latch is in hold mode, and the memory cell maintains the value of the latch data. Thus, the internal nodes are sensitive to soft errors.

In the proposed latch, two methods are used to harden the circuit:

1. Employing C-element based on which the output node changes when most middle nodes have the same logic.

2. Using the memory cell to maintain data.

This method increases the resistance of the output node and reduces its sensitivity to particle strike.

Essential parameters for the simulation in carbon nanotube technology using the Stanford model are presented in Table 1. The technology used in carbon nanotubes is 32 nanometers.

Table 1. *CNTFET model parameters.*

Parameter	value
The physical length of the channel	32.0 nm
Length of doped CNT source/drain expansions	32.0 nm
Fermi level of doped source/drain CNT regions	0.6 eV
The work function of source/drain metal contact	4.6 eV
CNT work function	4.5 eV
Mean free path in intrinsic CNT	200.0 nm
Mean free path in p+/n+ doped CNT	15.0 nm
Chirality of the tube	(25,0)
Sub-lithographic pitch	6.4 nm
Pitch (distance between two nanotubes)	20.0 nm
The dielectric constant of high-K gate oxide	16.0
The thickness of high-K gate oxide	4.0 nm

It should be mentioned that the simulation-based on CNTFET transistors uses the unique feature of CNTs, that is, the control of threshold voltage by a change in the diameter of the CNT. Therefore, by increasing the diameter of CNT, the threshold voltage is decreased the threshold voltage dissipation problem is relieved.

The sensitivity of digital circuits to high-energy particles strike, and the occurrence of faults due to SET and SEU, makes their design a difficult task. One of the technologies used to implement these circuits with high reliability is the CMOS technology. This technology is inherently capable of reconstructing the destroyed signals, but the reliability is reduced by moving towards nanometer circuits. The proposed hardened latch presented in this paper and the proposed circuit in CNT

technology can harden against high-energy particles.

Figure 7 depicts the SET masking capability of the proposed latch Circuit using CNT transistors. This figure shows the system clock, data input, and latch output by clk, D, and Q, respectively. Figure 8 shows the input-output timing diagram of the proposed hardened latch.

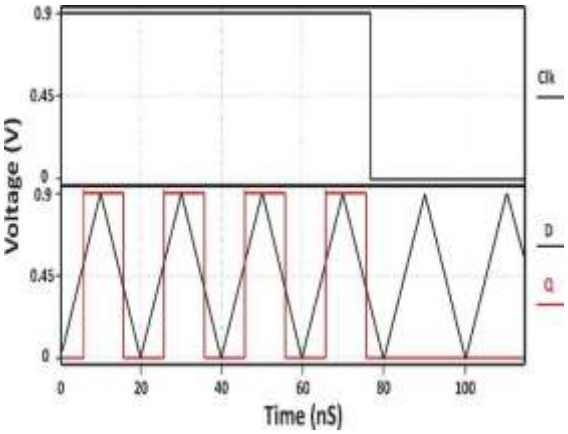

Figure 7. *SET filtering capability of the proposed latch using CNT transistors.*

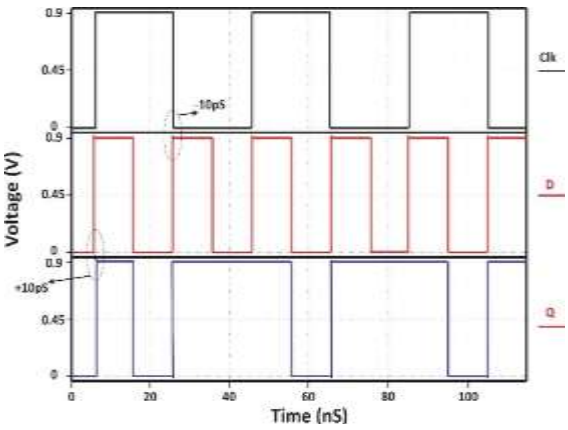

Figure 8. *Timing diagram of the proposed latch using CNT transistors.*

This section aims to extract the time parameters, including the rise time and the fall time of the proposed structure, along with their power consumption and area. In the following, the mentioned parameters are introduced for several latches, extracted in similar conditions, and compared with the proposed latch.

The time interval between the rising or falling edges of the input and output signal is measured to calculate the rise and fall times in the interval of the clock pulse signal where the latch is in the transparent mode. Table 2 shows the results of this simulation for the proposed latch and several sample latches. According to the obtained results in the proposed latch, the power consumption is lower than other simulated latches due to the lack of interaction between the nodes.

If the aim is to compare all three parameters of rising time, falling time, and power consumption, the resulting power-delay-product or PDP can be used. This quantity can be expressed in both PDP (max) and PDP (average) modes. In the first case, the maximum rise or fall time is multiplied by the power consumption, while in the second case, the average is taken from the fall time and rise time, and then the result is multiplied by the consumption power. The proposed structures have lower PDP than other simulated latches, which will result in higher efficiency and better performance. In this method, according to the specificity of the length and width occupied by the source and drain areas in these transistors and the number of known transistors of types P and N, the total area is obtained.

Figure (9-14) is the simulation results for the proposed latch.

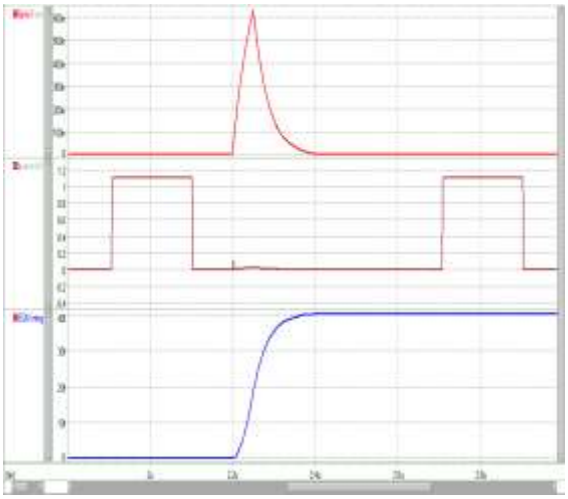

Figure 9. *A: Error modeling by exponential injection of additional current at middle node B: Latch output C: The*

amount of injected charge to the proposed latch.

Table 2 is a comparison of the proposed hardened latch with other similar latches. As can be seen, the proposed hardened latch has smaller area compared to other designs.

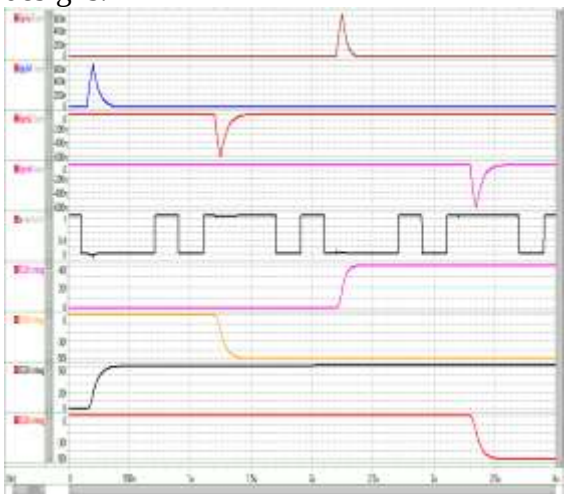

Figure 10. *Four types of injected charge to the latch and subsurface integration to calculate the amount of injected charge.*

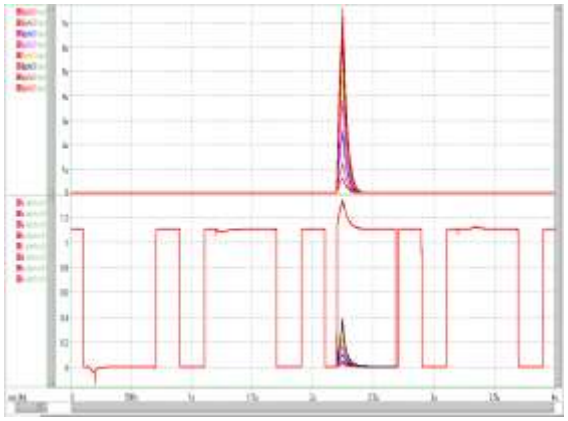

Figure 11. *Sweep the current to change the output bit.*

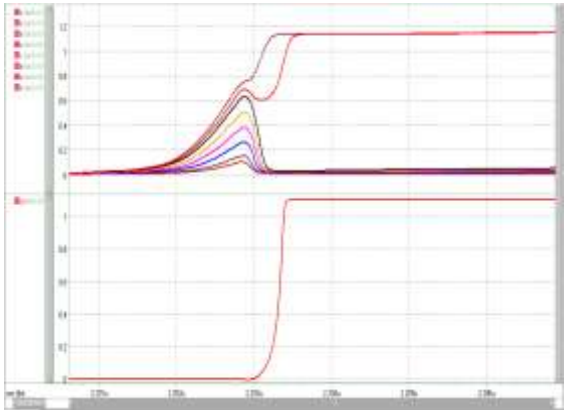

Figure 12. *The amount of injected charge up to the threshold of changes at latch output.*

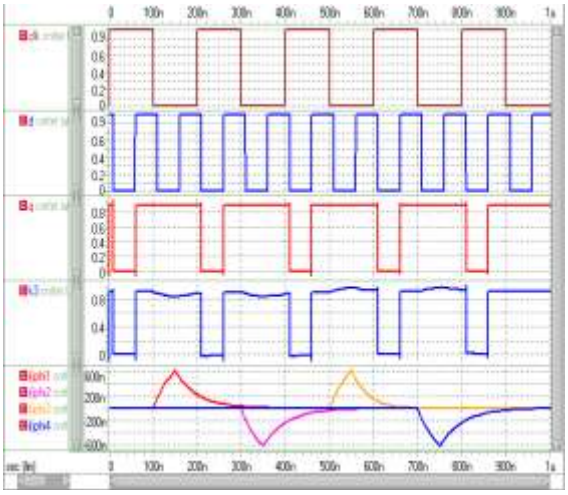

Figure 13. *Overall performance of the proposed latch and injected charges.*

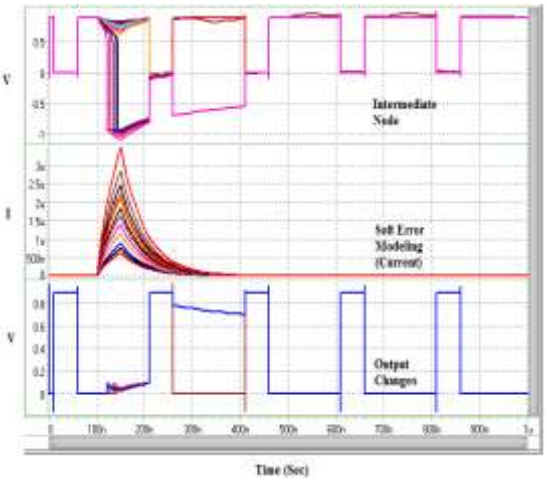

Figure 14. *The amount of soft error tolerance for the proposed latch.*

As shown in the simulation results, the CNTFET improves the circuit performance and resistance against transient faults. Therefore, the circuit is more robust compared to other existing technologies. It also reduces the power consumption and delay. In [40-41], experimental results for design and simulation results with ADS software is reported. In [42], analyze the effects of the parasitic elements of interconnection line is presented. As shown in Table 2, the main characteristic of the proposed latch has a low delay and low power consumption compared to other

similar latches. However, the proposed structures are more resistant to energetic particles strike than other similar structures.

Table 2. *Comparison of the parameters of the proposed latch design to several latches under the same simulation conditions.*

Parameters		Rise time(ps)	Fall time(ps)	Power (n watt)	(10^{-21}j)	(10^{-21}j)	Area (μm^2)
proposed latch (CNTFET) 32nm	For out =0	13.2	15.3	11.33	626.121	601	--
	For out=1	12.2	14.1	11.33	626	602	
proposed latch (CMOS) 180nm	For out =0	67	47	28.2	811.1	823.2	3100
	For out=1	63	44	28.2	812	822.1	
DICE [26]	For out =0	78.2	47.7	32.2688	2523.42	2031.321	14820
	For out=1	77.9	46.8	32.2688	2513.74	2011.96	
Latch in [30]	For out =0	89.1	85.3	11.0182	981.7216	960.787	14040
	For out=1	89.1	84.7	11.0182	981.7216	957.4816	
HiPeR in [37]	For out =0	25.3	15.4	10.3655	262.2472	210.9379	11700
	For out=1	25.4	15.3	10.3655	263.2837	210.9379	
HiPeR – CG [37]	For out =0	13	16.8	8.2820	139.1376	123.4018	13260
	For out=1	13.2	17.6	8.2820	145.7632	127.5428	
Latch in [38]	For out =0	71.5	96	7.2546	696.4416	607.5728	9360
	For out=1	71.5	95.4	7.2546	692.0888	605.3964	
SIN-LC [31]	For out =0	45.3	25.7	6.8177	308.8418	242.0284	5850
	For out=1	45.3	25.3	6.8177	308.8418	240.6648	
LSEH2 [39]	For out =0	247.9	146.4	28.3813	7035.724	5595.373	16380
	For out=1	277.3	145.2	28.3813	7870.134	5995.55	

The purpose of expressing the proposed structures resist single event transient (SET), especially single event upset (SEU). The proposed structure, which was expressed step by step, robust structures to single event transients were first proposed. The main difference between these structures and what has been presented in the articles is that they consume low power under the same resistance to energetic particles strike. Also, by maintaining this level of resistance of energetic particles strike, the power consumption and consequently the quantity of PDP is reduced.

Additionally, it has been tried to make the circuit as resistant as possible to single event upset (SEU),) so if the energetic particles affect even the output node and lead to a change in its logic, after a limited time, the output return to the before state and therefore mask the soft error.

4. CONCLUSION

The CNTFET inverters have a considerably higher intrinsic gain than their CMOS counterparts, making them very suitable for robust circuit designs. Also, the unique characteristics of the CNTFET device reduce most of the significant design limitations of the nanoscale CMOS technology. The proposed structures were proposed to prevent the soft errors caused by single event transient (SET) and multi event transient (SEU) problems. The principal characteristic of the proposed structure is lower power consumption and higher resistance to energetic particles strike compared to other similar latches. In other words, the proposed latch did not have any single node sensitive to the energetic particle strike, and the soft error caused by energetic particle strike to node-pairs and three sensitive nodes in them was masked with a suitable layout design.

To confirm the above mentioned, the proposed structure and several examples of

considered similar circuits by HSPICE software and in CMOS and CNTFET technology were simulated and compared.

The results showed that the proposed circuit has good performance in terms of speed and is more resistant to energetic particles strike than other similar structures.

REFERENCES

1. Knight, J. C., "*Safety critical systems: challenges and directions*", Proceedings of the 24th international conference on software engineering, (2002).
2. Constantinescu, C., "*Impact of deep submicron technology on dependability of VLSI circuits*", Proceedings International Conference on Dependable Systems and Networks, (2002).
3. Reviriego, P., Maestro, J. A., Cervantes, C., "Reliability analysis of memories suffering multiple bit upsets", *IEEE Transactions on Device and Materials Reliability*, **7**(4) (2007) 592-601.
4. Alioto, M., "Ultra-low power VLSI circuit design demystified and explained: A tutorial", *IEEE Transactions on Circuits and Systems I*, 59(1) (2012) 3-29.
5. Kim, Y.-B., "Challenges for nanoscale MOSFETs and emerging nanoelectronics", *Transactions on Electrical and Electronic Materials*, 11(3) (2010) 93-105.
6. Qi, C., "A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets", *IEEE Transactions on Device and Materials Reliability*, 16(3) (2016) 388-395.
7. NS, A. K. P., Baghini, M. S., "Robust soft error tolerant CMOS latch configurations", *IEEE transactions on computers*, 65(9) (2015) 2820-2834.
8. Seifert, N., Zhu, X., Massengill, L. W., "Impact of scaling on soft-error rates in commercial microprocessors", *IEEE Transactions on Nuclear Science*, 49(6) (2002) 3100-3106.
9. Baumann, R. C., "Radiation-induced soft errors in advanced semiconductor technologies", *IEEE Transactions on Device and materials reliability*, 5(3) (2005) 305-316.
10. Lee, H.-H. K., "Design framework for soft-error-resilient sequential cells", *IEEE Transactions on Nuclear Science*, 58(6) (2011) 3026-3032.
11. Islam, R., "*A highly reliable SEU hardened latch and high performance SEU hardened flip-flop*", Thirteenth International Symposium on Quality Electronic Design (ISQED), (2012).
12. Seifert, N., "*Radiation-induced clock jitter and race*", IEEE International Reliability Physics Symposium, Proceedings, 43rd Annual, (2005).
13. Chandra, V., Aitken, R.,."*Impact of technology and voltage scaling on the soft error susceptibility in nanoscale CMOS*", IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems, (2008).
14. Qi, C., "Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology", *Microelectronics Reliability*, 55(6) (2015) 863-872.
15. Kim, L. -S., Dutton, R. W., "Metastability of CMOS latch/flip-flop", *IEEE Journal of solid-state circuits*, 25(4) (1990) 942-951.
16. Omana, M., Rossi, D., Metra, D., "*Novel Transient Fault Hardened Static Latch*", ITC., (2003).
17. Shirinzadeh, S., Asli, R. N., "*A novel soft error hardened latch design in 90nm CMOS*", 16th CSI International Symposium on Computer Architecture and Digital Systems (CADS 2012), (2012).
18. Karnik, T., "*Selective node engineering for chip-level soft error rate improvement [in cmos]*", Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No. 02CH37302), (2002).
19. Harris, D., Weste, N., "*Cmos vlsi design*", ed: Pearson Education, Inc, (2010).
20. Peng, C., "Radiation-hardened 14T SRAM bitcell with speed and power optimized for space application", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 27(2) (2018) 407-415.
21. Li, Y.-Q., "A quatro-based 65-nm flip-flop circuit for soft-error resilience", *IEEE Transactions on Nuclear Science*, 64(6) (2017) 1554-1561.
22. Yan, A., "Novel Radiation Hardened Latch Design with Cost-Effectiveness for Safety-Critical Terrestrial Applications", *IEEE 28th Asian Test Symposium (ATS)*, (2019).
23. Mitra, S., "Logic soft errors: a major barrier to robust platform design", *IEEE International Conference on Test*, (2005).
24. Shivakumar, P., "*Modeling the effect of technology trends on the soft error rate of combinational logic*", Proceedings International Conference on Dependable Systems and Networks, (2002).
25. Baumann, R., "Soft errors in advanced computer systems", *IEEE Design & Test of Computers*, 22(3) (2005) 258-266.
26. Calin, T., Nicolaidis, M., Velazco, R., "Upset hardened memory design for submicron CMOS technology", *IEEE Transactions on nuclear science*, 43(6) (1996) 2874-2878.
27. Hazucha, P., "Measurements and analysis of SER-tolerant latch in a 90-nm dual-Vт CMOS process", *IEEE Journal of Solid-State Circuits*, 39(9) (2004) 1536-1543.

28. Stackhouse, B., "A 65 nm 2-billion transistor quad-core Itanium processor", IEEE Journal of Solid-State Circuits,.44(1) (2008) 18-31.
29. She, X., McElvain, K., "Time multiplexed triple modular redundancy for single event upset mitigation", *IEEE Transactions on nuclear science*, 56(4) (2009) 2443-2448.
30. Fazeli, M., "Low energy single event upset/single event transient-tolerant latch for deep subMicron technologies", *IET computers & digital techniques*, 3(3) (2009) 289-303.
31. Omana, M., Rossi, D., Metra, C., "Latch susceptibility to transient faults and new hardening approach", *IEEE Transactions on Computers*,.56(9) (2007) 1255-1268.
32. Iijima S. Helical, "Microtubulesof graphitic carbon", *Nature*, 354 (1991) 56.
33. Lin, S., Kim, Y.-B., Lombardi, F., "CNTFET-based design of ternary logic gates and arithmetic circuits", *IEEE transactions on nanotechnology*, 10(2) (2009) 217-225.
34. Deng, J., "*Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors*", Stanford University, (2007).
35. Akinwande, D. A., "*Carbon Nanotubes: Device Physics, RF Circuits, Surface Science, and Nanotechnology*", Stanford University, (2010).
36. Moaiyeri, M. H., "Design and evaluation of energy-efficient carbon nanotube FET-based quaternary minimum and maximum circuits", *Journal of applied research and technology*, 15(3) (2017) 233-241.
37. Omaña, M., Rossi, D., Metra, C., "High-performance robust latches", *IEEE Transactions on Computers*, 59(11) (2010) 1455-1465.
38. Glorieux, M., "New D-flip-flop design in 65 nm CMOS for improved SEU and low power overhead at system level", *IEEE Transactions on Nuclear Science*,.60(6) (2013) 4381-4386.
39. Rajaei, R., Tabandeh, M., Fazeli, M., "Low cost soft error hardened latch designs for nano-scale CMOS technology in presence of process variation", *Microelectronics Reliability*, 53(6) (2013) 912-924.
40. Marani, R., Perri A. G., "A Comparison of CNTFET and CMOS technology through the Design of a SRAM Cell", *ECS Journal of Solid-State Science and Technology*, 8(1) (2019) 1-18.
41. Marani, R., Perri, A. G., "Impact of Technology on CNTFET-based Circuits Performance", *ECS Journal of Solid-State Science and Technology*, 9(5) (2020).
42. Marani, R., Perri, A. G., "A Procedure to Analyze a CNTFET-based NOT gate with Parasitic Elements of Interconnection Lines", *International Journal of Nanoscience and Nanotechnology*, 17(3) (2021) 161-171.
43. Abhay S. Vidhyadharan, Vidhyadharan, S., "A novel ultra-low-power CNTFET and 45 nm CMOS based ternary SRAM", *Microelectron. J.*, 111 (2021) 105033.