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Short Communication

Novel Subtractor Design Based on Quantum-Dot Cellular Automata (QCA) Nanotechnology

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Abstract

Quantum-dot cellular automaton (QCA) is a novel nanotechnology with a very different computational method in compared with CMOS, whereas placement of electrons in cells indicates digital information. This nanotechnology with specifications such as fast speed, high parallel processing, small area, low power consumption and higher switching frequency becomes a promising candidate for CMOS technology. In this paper, a new architecture of Half and Full subtractor based on the QCA is proposed. We take advantage of optimal XOR gate in designing these arithmetic units, which has been already designed based on the QCA majority voter gate. Using this XOR gate in the architecture of designed arithmetic units in this paper, reduces number of used QCA cells to 55 and 136 for Half and Full subtractor, respectively. Proposed design is more efficient in terms of cell counts, covered area and delay, than the conventional subtractors based on the QCA. These subtractors are designed and simulated using QCA Designer 2.0.3.

Keywords*: Full subtractor, Half subtractor, Majority Voter (MV), Quantum dot cellular.*

1. INRODUCTION

CMOS technology scaling encounters serious problems such as short channel effects, power consumption, etc. Various efforts have been made to find new devices for replacing CMOS technology. QCA is a nanotechnology which can be implemented, in molecular or atomic size and it is smaller than CMOS. QCA technology is one approach for implementing logic circuits with specifications of small size, high clock frequency and low power consumption (Skotnicki et al., 2005). QCA cell consists of four quantum dots, which are located on the vertices of a square. There are two mobile electrons, which can move between dots inside cell (Ahmad et al., 2014 , Rahman et al., 2013). Electrons locate on the opposite corners of square in the ground state due to Columbic repulsion of like charges (Nejad et al., 2010). Part (a) of Figure 1, shows four quantum dots of QCA cell however parts (b) and (c) of this figure, depict two steady states for electrons which are used to represent binary '0' and '1'. If charge density on dot i is ρ_i, then cell polarization is defined as equation (1) (Tougaw and Lent, 1994).

A QCA cell has two types of polarization. If quantum dots 1 and 3 are occupied, polarization will be P = –1, which represents binary '0' and whenever electrons place in quantum dots 2 and 4, polarization will be P = +1 that stands for binary '1' (Lent and Tougaw, 1997 , Bahar et al., 2014).

$$P = \frac{(\rho 2+\rho 4)-(\rho 1+\rho 3)}{\rho 1+\rho 2+\rho 3+\rho 4} \qquad (1)$$

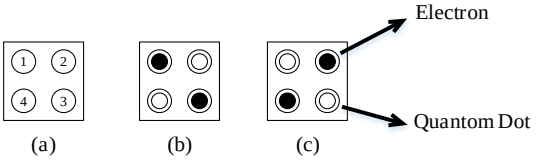

Figure1. *(a) Four quantum dots of QCA cell, (b) binary '0' and (c) binary '1'.*

We illustrate fundamental concepts of QCA circuits such as wire, inverter, majority gate and clocking in the following.
A QCA wire forms using an array of QCA cells as is shown in Figure 2.

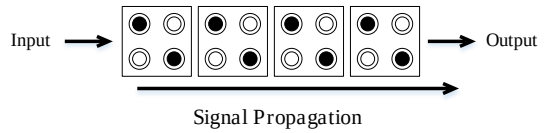

Figure2. *QCA wire*

Binary signals propagate from input to output because of the electrostatic repulsion between cells (Iakshmi et al., 2010). The simplest inverter is built placing QCA cells in a diagonal structure which is shown in figure 3(a). Polarization of "output" in this structure is opposite of "input" polarization. Figure 3(b) represents insusceptible to fault structure for a QCA inverter.

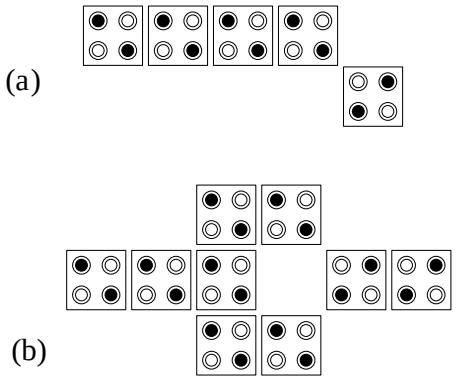

Figure3. *Two types of inverter, (a) simplest structure and (b) fault tolerant structure*

Majority gate is the fundamental unit of QCA-based design, which consists of five cells as follows, three input cells, one output cell and a center cell named device cell (Bahar et al., 2013). The center cell performs calculations. Figure 4 shows majority gate with input cells A, B, C and output cell F. Truth table for majority gate is shown in table 1. Equation (2) shows boolean expression for this gate.

$$Maj\ (A, B, C)=AB+AC+BC \quad (2)$$

Table1. *Truth table for Majority gate*

Inputs			**Output**
A	**B**	**C**	**F**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

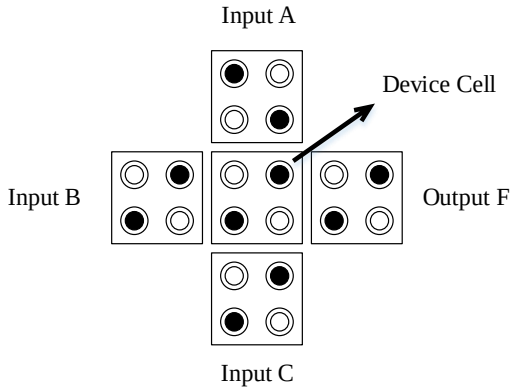

Figure4. *QCA Majority gate*

Logic gates such as AND, OR, NOT, etc can be implemented using majority gate. 2-input AND gate is realized by fixing one of three input cells to binary '0' while 2-input OR gate is formed applying fixed binary '1' to one of input cells.

Clocking is the main source of synchronization that plays an essential role in QCA circuits. A QCA cell requires four phases of clock, which are named as Switch, Hold, Release and Relax. During Switch phase, the inter-dot barriers in a zone are raised, while this occurs, electrons within cell can be influenced by the Columbic charges of neighboring zones. Then inter-dot barriers are kept up in the Hold phase, so that electrons do not switch between dots. Inter-dot barriers are reduced in the Release phase and cells lose their polarity. In the Relax phase, inter-dot

barrier is held down and a cell has no influence on its neighbors. Figure 5 represents a cell in its four clock phases (Hennessy and Lent, 2001 , Vankamamidi et al., 2006).

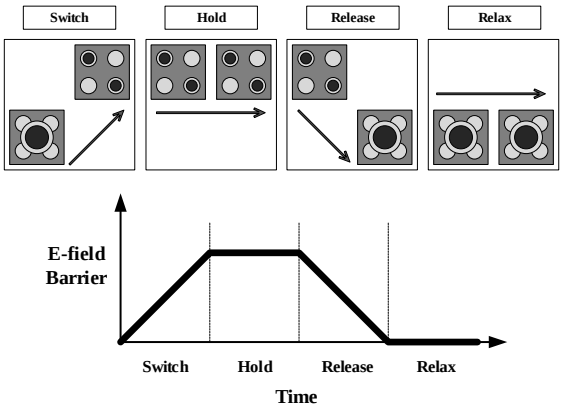

Figure5*. Four phases of QCA clock*

In this paper, a new architecture for Half and Full subtractor are proposed. In designing these arithmetic units, we employ optimal XOR gate, which has been reported before. Organization of this paper is as follows; In section 2, proposed QCA Half subtractor is demonstrated. Next, in section 3, a full subtractor is proposed and compared with other recent works which is followed by the conclusion in the last section.

Table2. *Truth table for Half Subtractor*

Inputs		Outputs	
A	**B**	**Borr**	**Diff**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

2. PROPOSED HALF SUBTRACTORS

Subtractor is one of the essential arithmetic units. A Half subtractor has two inputs A and B with two outputs of Diff (difference) and Borr (Borrow). It is a combinational circuit, which subtracts two bits. Diff shows subtraction results of inputs while Borr specifies if '1' has been borrowed. Equations (3) show Boolean expressions for Diff and Borr, moreover, truth table for a Half subtractor is shown in table 2.

$$\text{Diff} = \text{Difference} = A \oplus B \quad \& \tag{3}$$

$$\text{Borr} = \text{Borrow} = A'B$$

In our Half subtractor design, we exploit optimal XOR gate which has been already proposed (Skotnicki et al., 2005). Boolean expressions for XOR gate are shown in equation (4) and figure 6 shows this gate with the input cells A, B and the output cell XOR. This XOR has been implemented using 30 QCA cells.

$$\begin{aligned} XOR &= (A+B).(AB)' = \\ &(A+B).(A'+B') \\ &= AB' + BA' = A \oplus B \end{aligned} \tag{4}$$

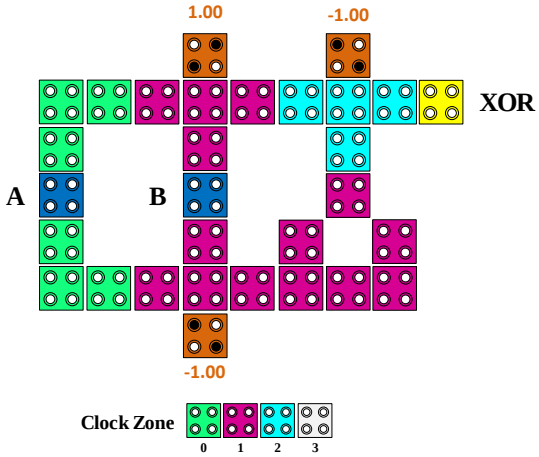

Figure6*. XOR gate based on QCA*

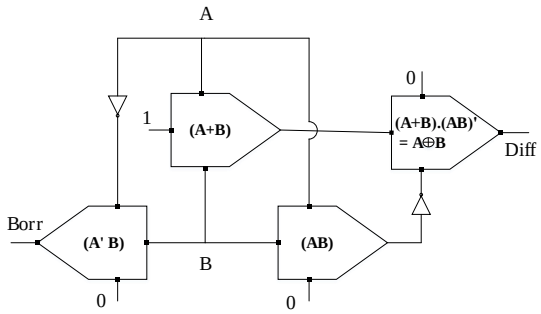

Figure7*. Schematic view of proposed Half subtractor*

Exploring mentioned XOR circuit reduces number of used QCA cells for the construction of Half subtractor. Figure 7 illustrates schematic view of the proposed Half subtractor.

As mentioned before, input cells are labeled with A and B while output cells are labeled with Diff and Borr. Figure 8 shows the QCA layout of proposed Half subtractor. In the last reported subtractor of ref (Akter et al., 2014), cell numbers are 70 however, in the proposed circuit, cell counts are 55 and this shows 21% reduction in the cell numbers. Covered area for the proposed circuit is 14×9 cells.

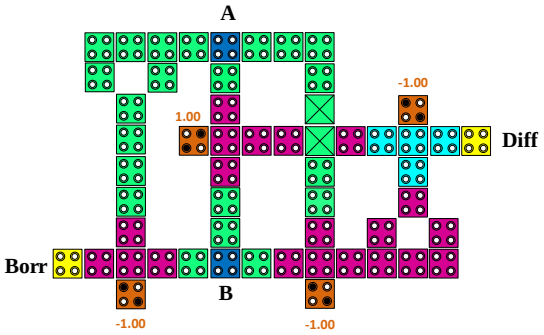

***Figure8**. QCA cell layout for the proposed Half subtractor*

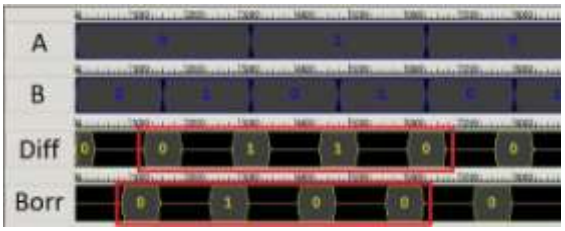

***Figure9**. Simulation results for the proposed Half subtractor based on QCA cells*

We exploit QCA Designer 2.0.3 for extracting different signals of the proposed Half subtractor. Figure 9 shows simulation results for this arithmetic unit.

All parameters are set at default values in this software. In QCA designer 2.0.3 cell size is 18 nm. Adding space between cells, this size increases to 20nm. Area is estimated based on the expression (5) which is 0.0504µm2 for designed half subtractor. Table 3 shows a comparison between proposed Half subtractors and existing subtractors.

$$\text{Area} = \text{maximum longitudinal cell numbers} \times \text{maximum transversal cell numbers} \times 400\text{nm}^2 \quad (5)$$

3. PROPOSED FULL SUBTRACTOR

A Full subtractor is a circuit, which subtracts two bits with considering the result of lower significant stage. Truth table for Full-subtractor is shown in Table 3, whereas A, B and C are inputs and Diff, Borr are outputs. Boolean expressions for Diff and Borr are shown in Equation (6).

$$\text{Diff} = A \oplus B \oplus C$$
$$\text{Borr} = A'B + (A \oplus B)'C \quad (6)$$

***Table3**: Truth table for Full Subtractor*

Inputs			Outputs	
A	**B**	**C**	**Diff**	**Borr**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

***Table4**. Comparison of proposed subtractors and conventional subtractors*

QCA Subtractor	Area(µm^2)	Cell count	Delay
Half Subtractor in [6]	16(cell)×14(cell)= 0.0896	77	3 clock phase
Half Subtractor in [2]	19(cell)×11(cell)= 0.084	70	4 clock phase
Proposed Half Subtractor	**14(cell)×9(cell) = 0.0504**	**55**	**3 clock phase**
Full Subtractor in [6]	(32cell)×16(cell) = 0.205	178	8 clock phase
Proposed Full Subtractor	**28(cell)×15(cell) = 0.168**	**136**	**7 clock phase**

We have designed a new module for Full subtractor and compared it with (Iakshmi

et al., 2010) design. Figure 10 illustrates a schematic view for the proposed Full subtractor whereas Figure 11 shows layout for this unit. The input cells are labeled with A, B and C while the output cells are labeled with Diff and Borr. There are 178 Cells in the Full subtractor of (Iakshmi et al., 2010) however in the proposed circuit, cell numbers are 136 and this shows nearly 24% reduction in the cell numbers. Covered area for the proposed Full adder is 28×15 cells which is 0.168μm^2 due to the expression (5).

Simulation results for this arithmetic unit are shown in Figure 12.

Table 4 shows a comparison between proposed subtractors and conventional ones. It is obvious from table 4 that proposed subtractors are more efficient in terms of cell counts, covered area and delay in comparison with their latest counterparts.

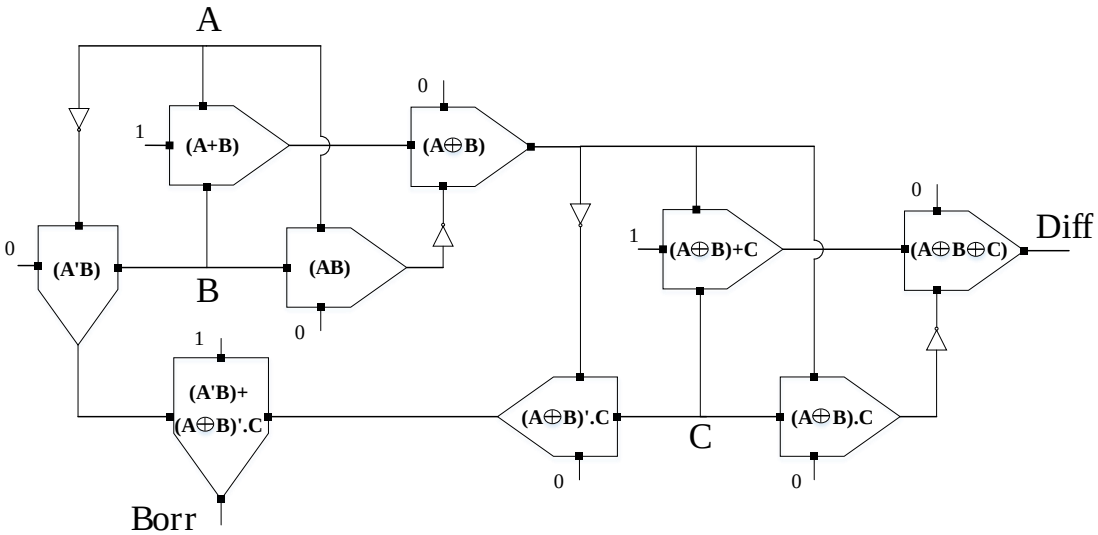

Figure10. *Schematic view of proposed Full subtractor*

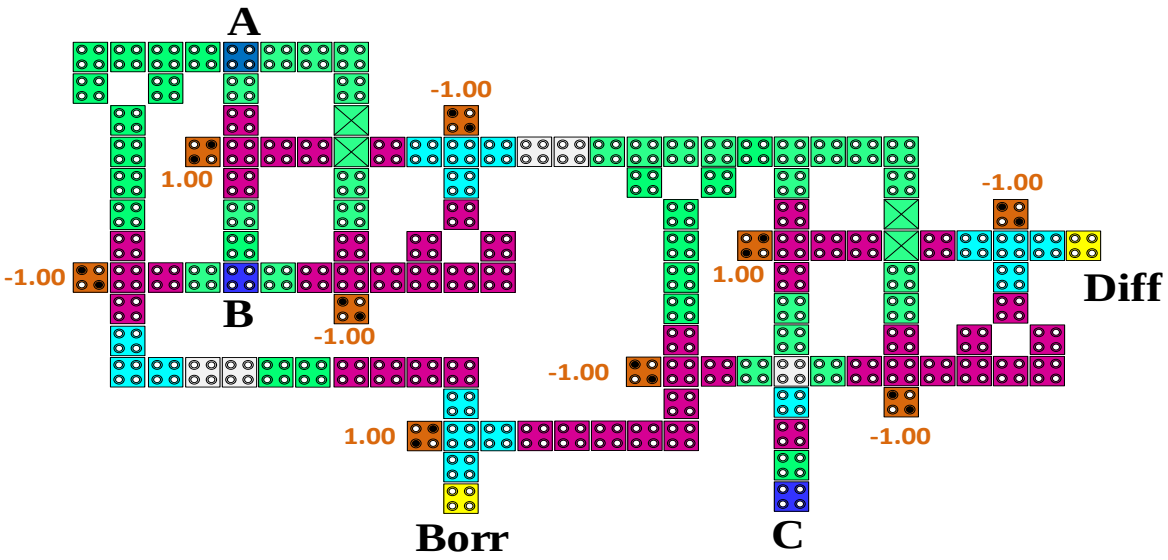

Figure11. *Layout for the proposed Full subtractor based on QCA cells*

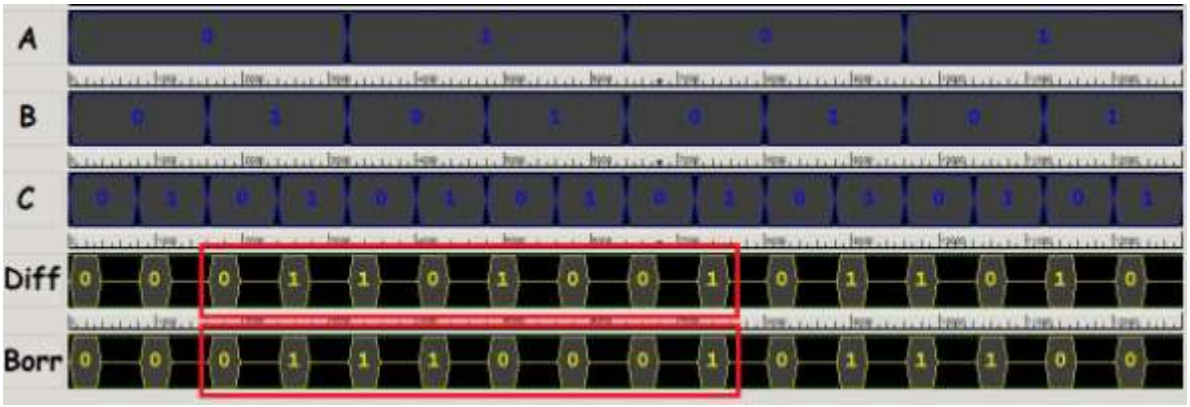

Figure12*. Simulation results for the proposed Full subtractor*

4. CONCLUSION

In this paper, a novel design of Half and Full subtractors based on QCA cell has been proposed. Using optimal basic gates such as optimal XOR in designing these circuits, tends to a considerable reduction in the used QCA cell numbers in comparison with the latest counterparts. Major specifications of these circuits are smaller cell numbers and subsequently smaller occupied area, lower delay and less power consumption. These specifications are of the great concerns in the arithmetic units.

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