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Imprecise Minority-Based Full Adder for Approximate Computing Using CNFETs

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Abstract

Nowadays, the portable multimedia electronic devices, which employ signal-processing modules, require power aware structures more than ever. For the applications associating with human senses, approximate arithmetic circuits can be considered to improve performance and power efficiency. On the other hand, scaling has led to some limitations in performance of nanoscale circuits. Accordingly, Carbon Nanotube Field Effect Transistors have gotten a widespread attention as the most appropriate replacement for MOSFETs. In this paper, an imprecise full adder cell based on CNFET minority gates is introduced. Evaluation and comparison of the minority-based and the-state-of-the-art imprecise full adders in terms of average power dissipation, delay and power delay product (PDP) are done. The error distance (ED), normalized error distance (NED) and PDP-NED product metrics are also considered for assessing the accuracy of the reviewed circuits. The HSPICE simulations, conducted using Stanford 32nm CNFET model, indicate that the minority-based design outperforms the other designs in terms of performance and error tolerance.

Keywords: *Approximate computing, Full adder, CNFET, Nanoelectronics.*

1. INRODUCTION

In the recent years, the energy efficiency has become a paramount concern in design of computing systems as they become increasingly embedded and mobile.

Computational functions of today's digital systems involve an expanded set of applications that encompasses media processes such as audio, video, and image processing. The limited perceptual capability of humans in construing images and videos, allows the outputs of media processing algorithms to be numerically approximate in preference to be accurate. Arithmetic units as a main infrastructure of media processor can be developed imprecise and provide further power saving compared to the conventional low-power design methodologies. Reducing area and delay in media processing systems is additional achievements of applying the approximation approaches.

Full adder cell as a basic building block of digital circuits especially media processors, plays a direct role in performance and broadly studied for approximate implementation [1, 2, 3, 4, 5, 6]. Scaling down the feature size deeper in nanoranges in Si-based MOS technology, leads to absolute limits on its performance because of appearing some problems such as short-channel effects, reduced gate control, exponentially rising leakage current, severe process variations and high power densities [7]. With careful evaluation of all potential emerging devices, ERD and ERM working groups recommended carbon based nano-electronics such as carbon nanotubes as a promising technology [8]. CNFET is the most encouraging option for replacing the Si MOSFET, because of its similarities with conventional MOSFET in terms of I-V characteristics and the existence of both

N-type and P-type transistors, which have led to comparable designing techniques with CMOS technology. In addition, CNFETs have a near-ideal combination of a high-mobility and ultra-thin body channel [9, 10, 11, 12, 13, 14 and 15].

The I-V characteristics for a bulk nMOS and an N-type CNFET with same gate widths at 32 nm technology node are illustrated in Figure 1. The results indicate that the CNFET device shows less short channel effects, has higher driving current and transconductance (gm), and experiences less mobility degradation.

The threshold voltage of a CNFET can be determined by adopting the proper diameter for its CNTs as shown in Equation (1). The diameter of CNT is a function of the chirality vector, which defined by (n1, n2) indices, and the relation is given by the Equation (2) [9].

$$V_{th} = \frac{0.436}{D_{CNT}(nm)} \quad (1)$$

$$D_{CNT} = 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

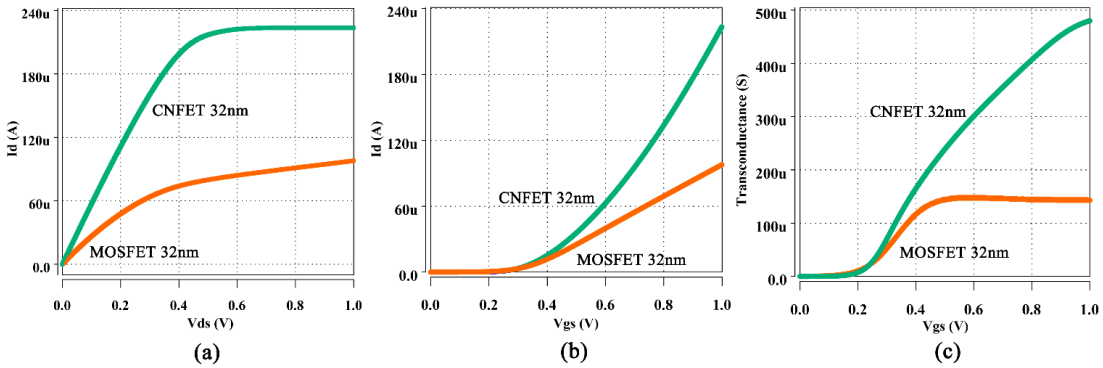

Figure 1. *The I-V characteristics of a 32nm MOSFET-like N-type CNFET (L=32nm, W=64nm (Tube=16, Pitch=4nm), (n1, n2)=(19,0)) vs. a 32nm NMOS (L=32nm, W=64nm) (a) Id-Vds (b) Id-Vgs (c) gm-Vgs [16].*

The rest of the paper is organized as follows: in Section 2, the existing imprecise full adders are reviewed. In Section 3, the minority-based approximate full adder is described. The simulation results and comparisons are given in Section 4. Section 5 investigates an image processing application for imprecise full adder and finally Section 6 concludes the paper.

2. THE EXISTING APPROXIMATE FULL ADDERS

In this section, the state-of-the-art imprecise full adder cells are reviewed [2, 3, 4]. It is worth mentioning that the previous MOSFET-based designs have been modified and optimized for 32nm CNFET technology.

The first imprecise FA (IFA1) is an approximation structure of conventional CMOS mirror adder as shown in Figure 2.

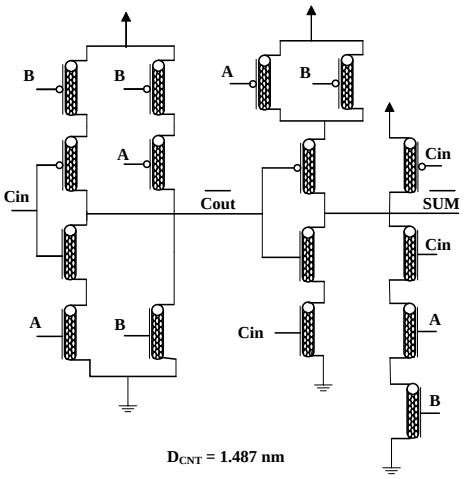

Figure 2. *Imprecise full adder 1 (IFA1)*

Obviously, this circuit has eight fewer transistors compared to the conventional

full adder cell. There is one error in *Cout* and two errors in *SUM* in IFA1.

The second imprecise full adder (IFA2) is shown in Figure 3. Structure of IFA2 is based on the fact that *SUM* is inverse of *Cout* signal in six out of eight cases. *SUM* has only two errors, while *Cout* is correct for all combinations of input signals.

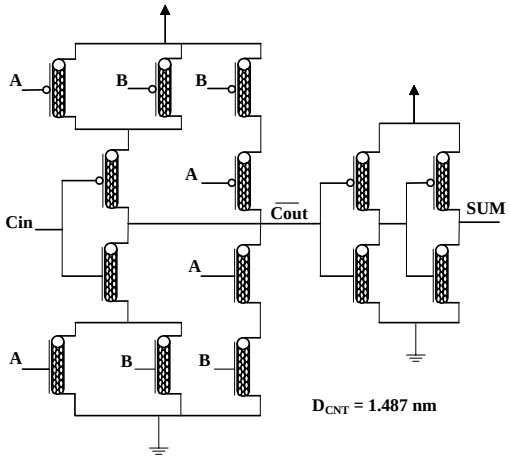

Figure 3. *Imprecise full adder 2 (IFA2).*

By combining IFA1 and IFA2, more transistors can be eliminated from the conventional design, which is resulted in imprecise FA3 (IFA3). This structure has one error in *Cout* and three errors in *SUM*. Figure 4 depicts the schematic of IFA3.

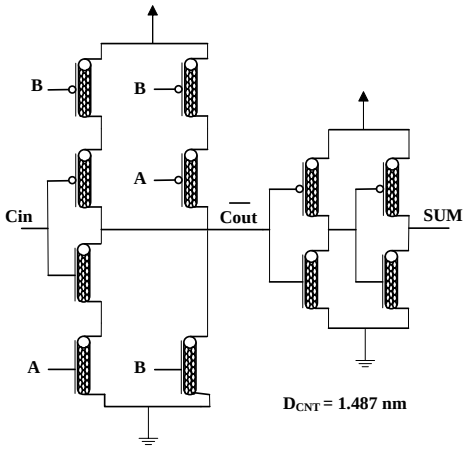

Figure 4. *Imprecise full adder 3 (IFA3).*

The truth table of the exact FA shows that the *Cout* signal is equal to the A signal and also equal to the B signal for six out of eight terms. Therefore, in imprecise FA4 (IFA4), *Cout* is considered as A due to the interchange relation between A and B signals. This design utilized an inverter to calculate $\overline{Cout}$, and *SUM* signal generates from $\overline{Cout}$ similar to IFA1. This structure has two errors in *Cout* and three errors in *SUM*. Figure 5 is illustrated IFA4.

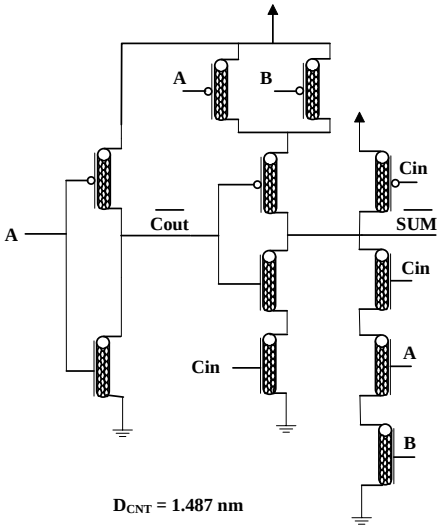

Figure 5. *Imprecise full adder 4 (IFA4).*

The imprecise 8-transistor XNOR-based FA5 (IFA5), which is shown in Figure 6, is designed based on 10-transistor full adder in [17]. *SUM* signal of an accurate FA, is equal to *Cin* signal in half of the input signals combinations, so the functions of *SUM* and *Cout* are considered as Equations (3) and (4), respectively. In IFA5, both *SUM* and *Cout* are correct for four out of the total input combinations.

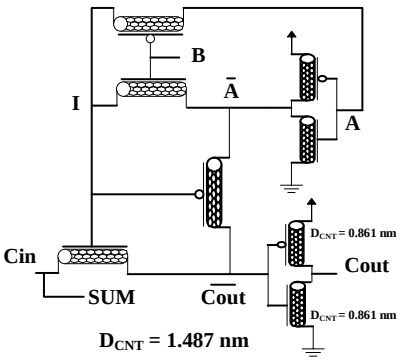

Figure 6. *Imprecise full adder 5 (IFA5).*

$$SUM = C_{in} \tag{3}$$

$$C_{out} = \overline{(A \oplus B)C_{in} + \bar{A}\bar{B}} \quad (4)$$

Imprecise FA6 (IFA6) with six transistors is approximate structure of accurate design in [18], which its functions of *SUM* and *Cout* are given by Equations (5) and (6) respectively:

$$SUM = \overline{A \oplus B} \quad (5)$$

$$C_{out} = (A \oplus B)C_{in} + AB \quad (6)$$

SUM signal is accurate for half of the eight input combinations, while *Cout* is accurate. The schematic of IFA6 in Figure 7 expresses that this circuit has four fewer transistors as compared to the accurate one.

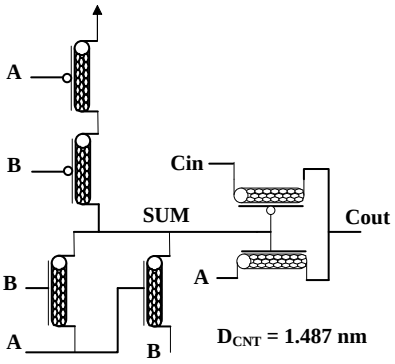

Figure 7. *Imprecise full adder 6 (IFA6).*

Imprecise XNOR-based FA7 (IFA7), shown in Figure 8, is an extension of IFA6, with two more pass transistors to improve the accuracy of *SUM* signal. In this structure, *SUM* has only two errors, while *Cout* is accurate for all the possible combinations. The functions of *SUM* and *Cout* signals are as Equations (7) and (8), respectively:

$$SUM = \overline{(A \oplus B)}C_{in} \quad (7)$$

$$C_{out} = (A \oplus B)C_{in} + AB \quad (8)$$

The other imprecise full adder (IFA8) based on CNFET is proposed in [4]. That proposal is designed based on NAND and NOR structure with 12 transistor.
SUM signal is accurate for six of the eight input combinations, while Cout is accurate. Functions of *SUM* and *Cout* are given by Equations (9) and (10) respectively:

$$SUM = \bar{A}.(\overline{B.C}) + A.(\overline{B+C}) \quad (9)$$

$$C_{out} = \overline{SUM} \quad (10)$$

An imprecise full adder cell has also been suggested in [19]. However, in this cell the *Cout* output is not full-swing and it has 0V and VDD/3 as ‘0’ and 2VDD/3 and VDD as ‘1’. As a result, this cell requires additional gate to complete the voltage level of the *Cout* signal and is suitable for blocks such as serial adders. Moreover, in this work important applications of imprecise adders such as image processing have not been investigated.

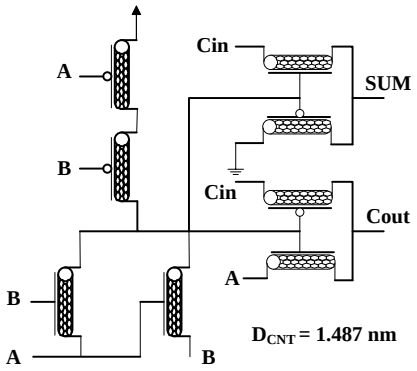

Figure 8. *Imprecise full adder 7 (IFA7).*

3. THE MINORITY-BASED APPROXIMATE FULL ADDER

The minority based imprecise FA is illustrated in Figure 9. This cell is a simplified implementation of the exact FA of [20]. Conventional methods for implementing minority gate require more transistors and subsequently have higher power, delay and area. The minority gate includes input capacitors and a complementary FET inverter. Capacitor network is used to provide voltage division and the inverter is used to implement minority logic. In a three-input minority gate, four different voltages (0, VDD/3, 2VDD/3 and VDD) appear in the gate of the inverter which is due to the voltage division between the capacitors. When the divided voltage in the gate of the inverter

is 0v (all inputs are low) or 0.3v (only one of the input signals is high) according to the Voltage Transfer Characteristic (VTC) of the inverter, the output of the minority gate is high (VOH=0.9v). For other input combinations, divided voltage in the gate of the inverter is equal to 0.6v (two out of three input signals is high) or 0.9v (all of the input signals are high) and in keeping with VTC of the inverter, the output of the minority gate is low (VOL=0v).

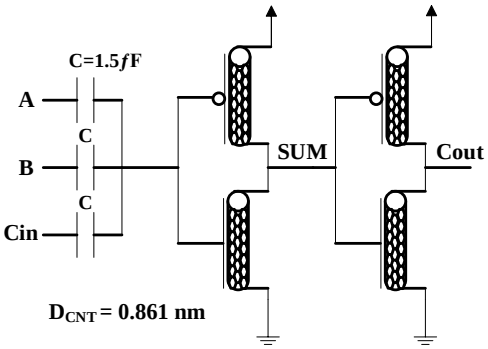

Figure 9. *The minority-based imprecise FA.*

The small gate capacitance of the CNFET-based inverter is ignorable as compared to the input capacitors and does not affect the voltage level of the inverter's input [21, 22]. It is notable that the utilized CNFET model in [21, 22] considers the gate and parasitic capacitances for simulations. It is also worth mentioning that implementing capacitors using CNFET transistors has been reported in [23]. Moreover, designing circuits based on capacitors and CNFETs has already been reported in [24]. It is worth mentioning that, in the CNFET technology wire capacitance can be reduced by replacing Cu interconnect with CNT bundle interconnect, and it is possible to obtain low voltage swing driving a wire with a capacitor [23].

Figure 10 demonstrates the voltage transfer characteristic (VTC) of the CNFET inverter. As compared to the 32nm MOSFET, 32nm CNFET has a quite sharper curve in the transition region due to the higher gain, which contributes considerable improvement in Noise Margin [25]. This considerably sharp transition region is due to the very high intrinsic voltage gain of the CNFET inverter. As illustrate in Figure 1, CNFET has considerably higher *gm* and small signal resistance at the saturation region (*ro*) and consequently very higher intrinsic gain as compared to MOSFET. Nanoscale MOSFETs suffers from severe short channel effects, degraded mobility and velocity saturation, which degrade the intrinsic gain. The aforementioned benefits of CNFET make it more suitable for being utilized in minority structures.

The minority-based imprecise FA follows a similar logic with IFA2, which is expressed before. However, in the minority-based imprecise structure, a minority gate replaces the *SUM* generator circuit of IFA2 structure as depicted in Figure 9. Therefore, the two-transistor path for charge and discharge of the *SUM* node is decreased to one transistor. On the other hand, the branches on the *SUM* node in the minority-based imprecise FA are less than IFA2, which leads to lower power dissipation and delay. To generate the exact *Cout* function of the minority-based imprecise FA, an inverter is placed after *SUM*. In this structure, *SUM* has only two errors, while *Cout* is accurate for all input combinations.

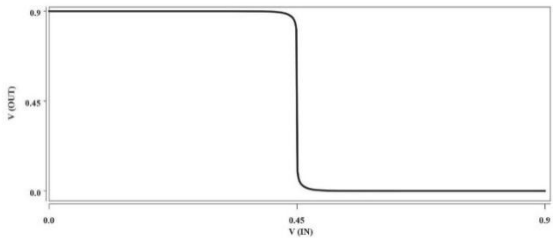

Figure 10. *The VTC of CNFET Inverter (DCNT=0.861 nm).*

4. SIMULATION RESULTS

Performance validation of each imprecise full adder (IFA) design has been pursued in terms of average power dissipation, delay, and power delay product (PDP) [26]. The SPICE simulations have been performed on the investigated imprecise full adders using the

Stanford HSPICE Model for 32nm CNFET technology [21, 22]. This standard model for enhancement-mode MOSFET-like CNFET considers a pragmatic and circuit-compatible device structure for HSPICE simulations. This model includes realistic device nonidealities and parasitics such as inter-CNT charge screening effects, quantum confinement effects on both circumferential and axial directions, Schottky-barrier effects at contacts, finite scattering mean free path, doped source/drain regions and parasitic capacitance and resistance. Furthermore, it considers a full transcapacitance network for more precise transient performance simulations with HSPICE. This CNFET model has already been widely used for simulation of different types of CNFET-based circuits in many valid references such as [9, 11, 12, 13, 14, 15, 16, 27 and 28].

The transient response of the minority-based IFA, considering all 64 possible input transitions, is demonstrated in Figure 11, which indicates the correct and proper operation of this design.

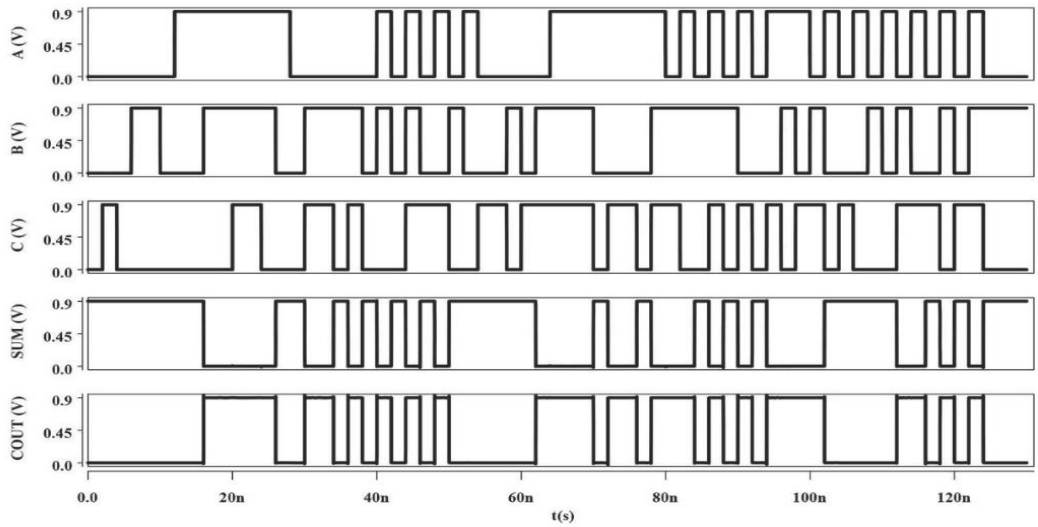

Figure 11. *Transient response of the minority-based IFA.*

Some precision evaluation metrics such as Error Distance (ED), Mean Error Distance (MED) and Normalized Error Distance (NED) that introduced in [29] are used to evaluate approximate designs.

Error distance (ED) is defined as the arithmetic distance between an erroneous output and the precise one. Total error distance (TED) is the sum the EDs for all the inputs of each full adder cell. The mean value of the EDs of all possible outputs is MED (Equation (11)), that is useful in evaluating the efficiency of an approximate implementation. Normalized error distance, referred to as NED, is used in characterizing the reliability of an approximate design (Equation (12)).

$$MED = \sum_i ED_i * p_i \qquad (11)$$

$$NED = \frac{MED}{D} \qquad (12)$$

where p_i the probability of ith input, and D is the maximum amount of error that an imprecise adder can take. In addition, the PDP-NED product is reported to investigate the power and precision tradeoff of approximate designs.

Table 1 illustrates the performance summary of the imprecise full adder cells. The minority-based design has the lowest average power consumption and PDP. IFA4 has the shortest propagation delay among other designs. In evaluating the reliability of IFAs, the minority-based IFA has the minimum total error distance as well as IFA1, IFA2, IFA7 and IFA8 designs. However, the minority-based

design has significantly lower PDP-NED product that specifies the efficacy of this design in trading off the accuracy for power. Since all previous designs were simulated with CNFET, Superiority of the proposed design is due to the approximate computing.

For the sake of completeness, the performance of the proposed imprecise full adder is also compared with accurate adder cell [30]. This is simulated under the same conditions described before. The comparisons are shown in Table 2, where the superiorities of the proposed imprecise design are clearly visible in terms of power and PDP.

To evaluate the sensitivity of the circuits to the temperature variation, the temperature varied from 0 to 90 ˚C for proposed design and the IFA3 that had the best PDP compared to other designs. The results for PDP are shown in Figures 12. As it can be seen PDP of the proposed circuit, are less affected by temperature variations as compared to the other design.

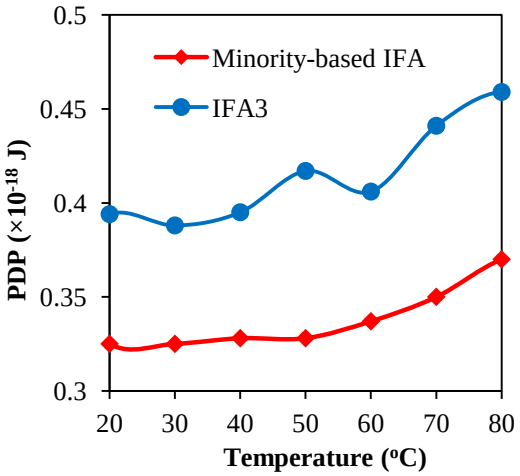

Figure 12. *PDP variation against temperature variations.*

Table 1. *Performance comparison of the imprecise full adder cells.*

IFA cells	Power (nW)	Delay (ps)	PDP (aJ)	TED	NED	PDP × NED
IFA1	76	7.86	0.597	2	0.083	0.050
IFA2	72.7	7.29	0.531	2	0.083	0.044
IFA3	59.1	6.68	0.395	3	0.125	0.049
IFA4	76.4	6.55	0.500	3	0.125	0.062
IFA5	219	80.4	17.6	4	0.166	2.921
IFA6	20.4	30.3	0.618	4	0.166	0.103
IFA7	28.4	76.2	2.16	2	0.083	0.179
IFA8	250.3	6.57	1.65	2	0.083	0.137
Minority-based IFA	**16.1**	**20.4**	**0.329**	**2**	**0.083**	**0.027**

Table 2. *Simulation results (proposed versus exact full adders).*

Design	Power (nW)	Delay (ps)	PDP (aJ)
Exact FA	3148.4	6.73	21.2
Minority-based IFA	**16.1**	**20.4**	**0.329**

5. APPLICATION

In this section, the application of the imprecise full adders is investigated in image multiplication. Partial products in multiplication are reduced with IFA cells and then these imprecise multipliers are compared with exact multiplier, which is reduced using exact full adder cells.

RGB (Red Green Blue) pixel values are numbers between [0, 255], so 8 bits are required for displaying each pixel; therefore 8×8 multiplication is performed for this application. It is worth noting that the image multiplying is performed using C++ language simulated in Microsoft Visual Studio 2012.

The result of a pixel-by-pixel multiplication is an image that each RGB value of its pixels is obtained by multiplying two input images, and then the reduction stage is done using the imprecise and exact full adders. Figure 13 illustrates a 8×8 multiplier, where the partial products that are produced in the first stage multiplications, are reduced using full adder cells. In fact, in this type of multiplication, the full adders are cascaded in some levels, videlicet; the outputs of the full adders are used as the inputs of the next level full adders.

To identify the quality of the output image of the imprecise multiplier based on the minority-based imprecise FA and compare it with the output images of other imprecise and exact multiplier, the peak signal-to-noise ratio (PSNR) are measured and illustrated in Table 3.

Table 3. *PSNR result of two image multiply examples.*

Image processing results	PSNR
IFA1	(28.38, 29.34, 29.28)
IFA2	(23.18, 20.31, 21.66)
IFA3	(19.62, 18.23, 19.10)
IFA4	(25.35, 23.68, 24.49)
IFA5	(20.26, 19.35, 18.52)
IFA6	(23.30, 22.11, 23.40)
IFA7	(21.95, 25.13, 24.44)
Minority-based IFA	(23.18, 20.31, 21.66)

PSNR measures the quality of the inexact output compared to the output of an exact multiplying.

For each example, PSNR values are represented with a three-valued vector that each index determines the PSNR of one of the RGB colors. According to Table 3 and the results of the image multiplying shown in Figure 14, the output image of the minority-based inexact multiplying has an acceptable quality as compared to the other inexact multiplying results. Moreover, as shown before in Table 1, it consumes considerably lower power. As a result, the minority-based imprecise cell can be used in image processing applications to reach an efficient design.

6. CONCLUSION

A minority-based imprecise full adder with a simple circuit structure has been investigated in this paper. The simulations have been carried out using 32nm CNFET HSPICE model to evaluate the average power, delay and power delay product (PDP). The total error distance, normalized error distance and PDP-NED product metrics are also deliberated for evaluating the reliability of reviewed circuits. The application of these imprecise full adders in image processing is investigated and the PSNR of the output images is reported to determine the quality of the images. The minority-based full adder is superior in terms of performance, accuracy and error tolerance as compared to other modern imprecise FAs, recently introduced in the literature.

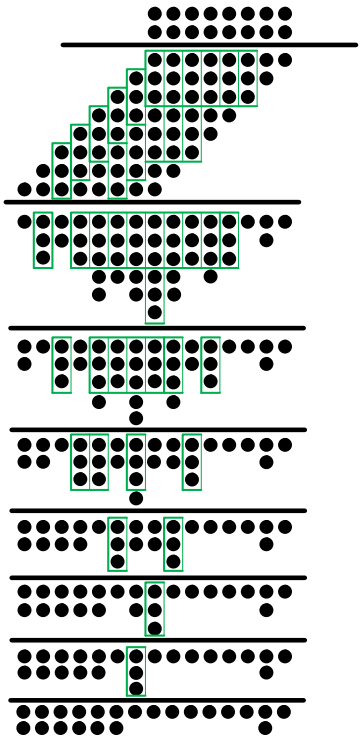

Figure 13. *Reduction steps using full adder cells.*

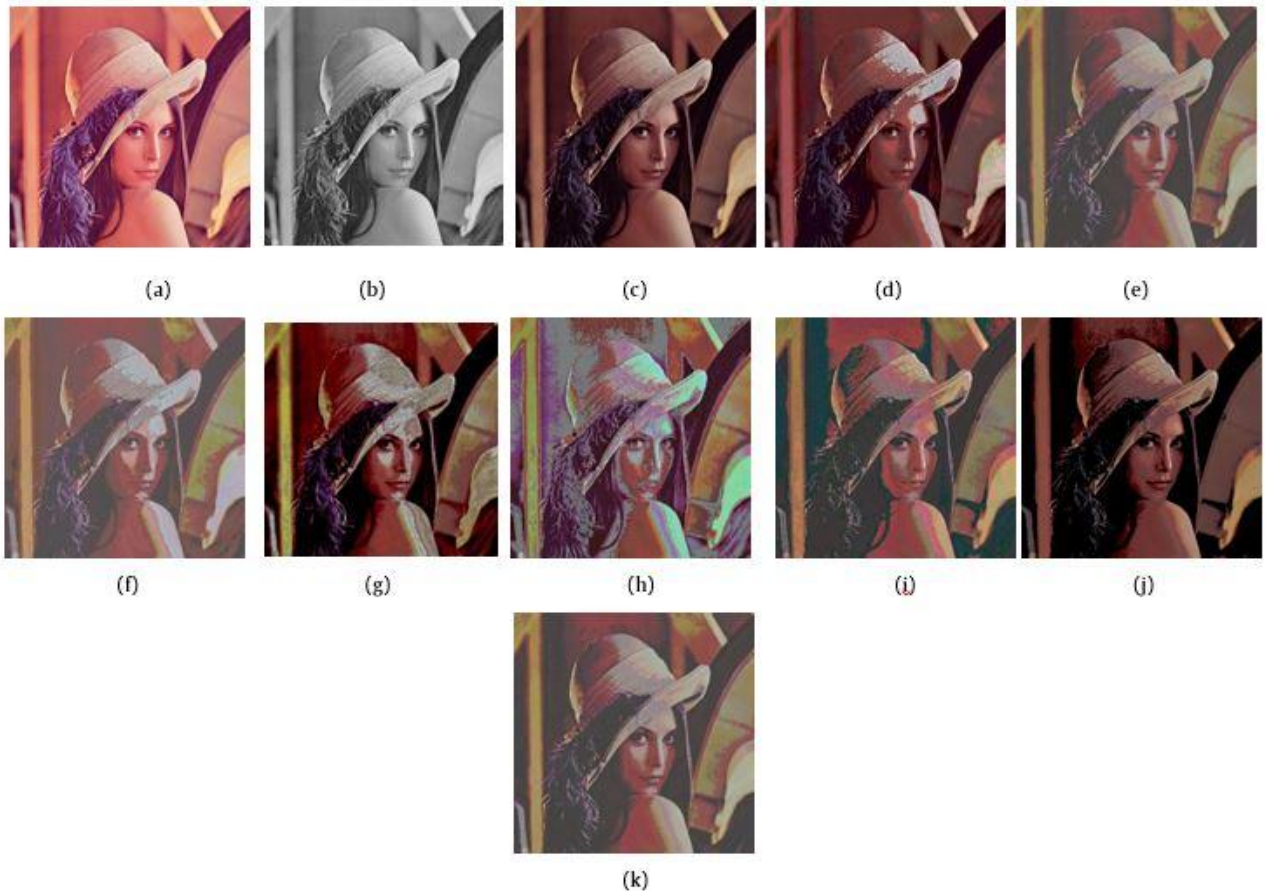

Figure 14. *Image multiplication results: (a) First input, (b) Second input, (c) Exact result, (d) IFA1, (e) IFA2 , (f) IFA3, (g) IFA4 , (h) IFA5 , (i) IFA6 ,(j) IFA7 , (k) Minority-based IFA.*

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