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Design and simulation of ternary logic circuits using CNTFETs

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Abstract

This paper shows how Carbon Nanotubes FETs (CNTFETs) can be used in the design of ternary logic gates, which is a promising alternative to the conventional binary logic design. In particular we propose a procedure to design some CNTFET-based logic gates, all in ternary logic, where all simulations are performed in Verilog-A, avoiding so the problems presented in SPICE.

Keywords: CNTFET, Modeling, Ternary Logic Circuits, Advanced Device System (ADS), Verilog- A

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1. Introduction

Carbon Nanotube Field Effect Transistors (CNTFETs) are a new kind of molecular device, using a carbon nanotube as channel [1-8].

For MOSFET-like CNTFETs in [2-17] we have already proposed a compact, semi-empirical model of CNTFET, implemented to carry out static and dynamic analysis of analogue and digital circuits [18-19], obtaining a significant improvement compared to Wong model [20-22].

In this paper we want to show the potentiality of the CNTFETs in the design of ternary logic gates.

In particular we propose a design technique of some CNTFET-based logic gates, all in ternary logic, using the complete model structure and the dynamic complex gate design as in [23].

The simulations are obtained in Verilog-A [24], contrary to the previous designs, proposed in literature, which use SPICE [23, 25]. Indeed the novelty of this article is that for the first time a comprehensive Verilog-A-based simulation for ternary logic gates using CNTFETs is proposed.

The presentation of the paper is organized as follows. At first, we briefly recall our CNTFET model. Then we design the ternary logic gates based on CNTFETs, showing and discussing the obtained results, together with conclusions and future developments

2. A BRIEF REVIEW OF OUR CNTFET MODEL

An exhaustive description of our CNTFET model is in [2-3]. Therefore, we suggest that the reader to consult these references.

It is a compact, semi-empirical model directly implementable and easy to use in simulation software to design analog and digital circuits: in fact, the most complex part of the model is contained in Verilog-A. In particular, the simulation has been run using Advanced Design System (ADS), which is also accepts devices described by a model written in Verilog-A. We have considered a single-wall n-CNTFET under the ballistic transport assumption. This assumption allowed us to define an analytical formula for CNT current.

When a positive voltage V_{GS} is applied between gate and source, the conduction band at the channel beginning decreases by qV_{CNT}, where q is the electron charge, and V_{CNT} is the surface potential.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed using the Landauer formula [26]:

$$I_{DS} = \frac{4qkT}{h}\sum_p \left[\ln\left(1+\exp\xi_{Sp}\right) - \ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

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where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, and p is the number of sub-bands.

ξ_{Sp} and ξ_{Dp} have the following expressions [2-3]:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT}$$

and

$$\xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \quad (2)$$

where E_{Cp} is the sub-bands conduction minima, V_{DS} is the drain-source voltage, and V_{CNT} is the surface potential.

In [2], we have proposed to evaluate V_{CNT} using the following approximation:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \frac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \frac{E_C}{q}\right) & \text{for } V_{GS} \geq \frac{E_C}{q} \end{cases} \quad (3)$$

where E_C is the conduction band minimum for the first sub-band and α is a parameter depending on V_{DS}, CNTFET diameter, and gate oxide capacitance C_{ox} [2-3].

Moreover, the proposed analytical modelling equations describing the current transport in CNTFETs were developed from physical electronics [27-28].

In order to correctly simulate the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

We have achieved this goal using an empirical method [2-3], more suitable for simulations in a CAD environment.

This method requires the extraction of the previous parasitic elements by comparing the device characteristics with the measured ones.

In this way, all elements of the equivalent circuit in Figure 1 can be determined.

It is similar to a common MOSFET one and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD}, the inductances of the CNT L_D and L_S, and the resistors R_D and R_S, in which the parasitic effect due to the electrodes is also included.

Figure 2 shows the output I-V characteristics of the CNTFET under test.

In the following simulations, our model has been translated into the programming language Verilog-A and then implemented on the simulator Advanced Design System (ADS).

3. REVIEW OF TERNARY LOGIC

A ternary function f (X_1, X_2, ..., X_n) is defined as a function mapping $\{0, 1, 2\}^n \rightarrow \{0, 1, 2\}$.

The three basic operations are:

$X_a + X_b = \max\{X_a, X_b\}$

$X_a \bullet X_b = \min\{X_a, X_b\}$

$\bar{X}_i = 2 - X_i$

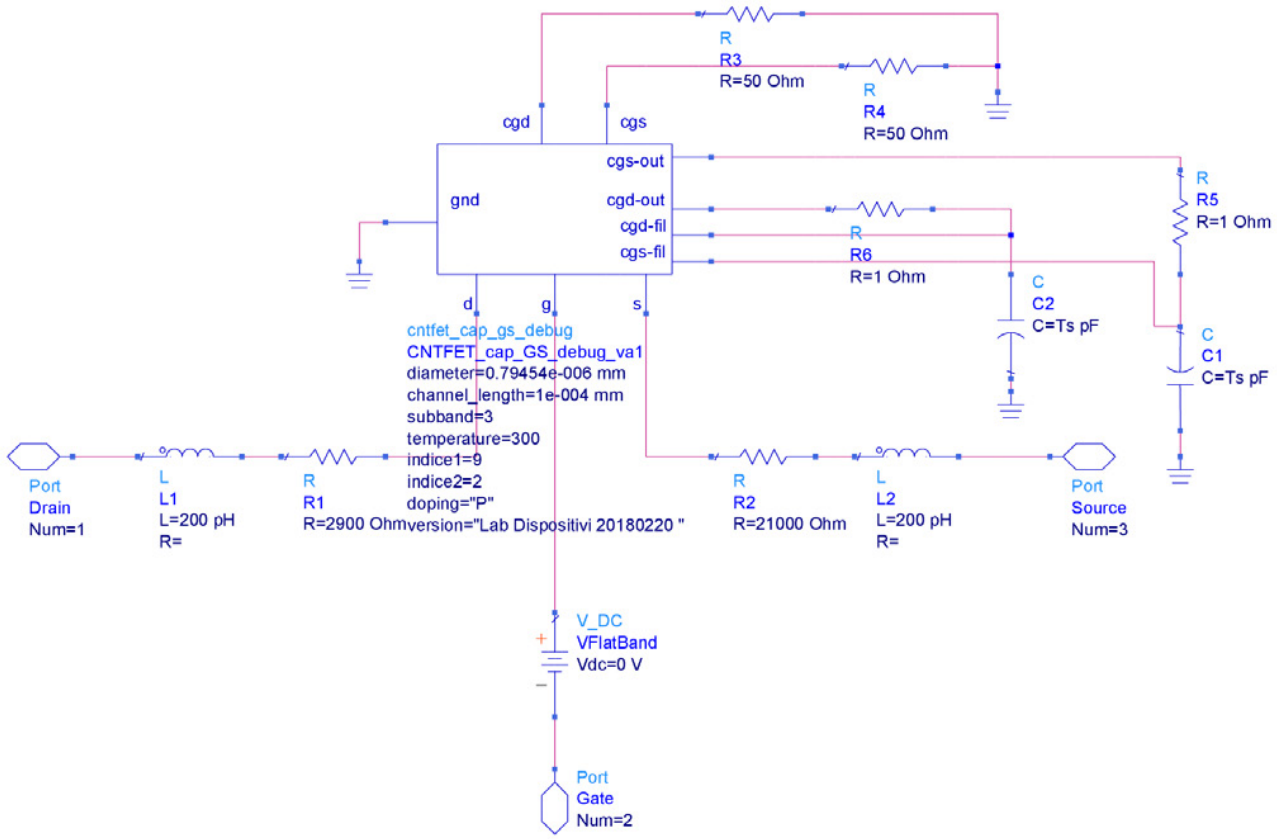

Figure 1. Verilog-A model of a n-type CNTFET in ADS [4].

where + is the OR, ● is the AND, and denotes the NOT in ternary logic. The ternary logic NOT is a gate with one input and three outputs as described in Table 1, where NTI is the negative ternary inverter, STI is the standard ternary inverter, and PTI is the positive ternary inverter [25].

Ternary NOR and NAND are thus easily described by the following expressions:

$$NOR\ (X_a, X_b) = \max\{X_a, X_b\}$$

$$NAND\ (X_a, X_b) = \min\{X_a, X_b\}$$

The truth table for the NOR and the NAND is shown in Table 2.

A ternary dcoder is a combinational circuit with one selection input S (SEL) and three outputs (X_0, X_1, and X_2), as shown in Table 3.

The first is a combinational circuit with three inputs (I0, I1, and I2) besides a selection input (SEL) and one output (OUT), as shown in Table 4.

The second circuit is built like a binary flip-flop. It clearly delivers three logic levels, and it is called flip-flop because of this.

4. Experimental set-up and methodology

4.1. Ternary NOR gate design

As shown in [23], a precharge signal (indicated as PRE in Figure 3) is needed as a binary-to-ternary interface that allow the design of the ternary logic gates without different threshold voltages for CNTFETs.

It works with two power supplies: VDD = 0.9 V and VDDL = VDD/2 = 0.45 V, as shown in Figure 3.

When PRE is high, the output node is pre-charged to VDDL by CNT11, and transistors CNT7 and CNT3 are on. Thus, CNT4 and CNT8 are both off. When PRE is low, CNT11 is turned off while CNT4 and CNT8 are turned on, letting the inputs pass through them to CNT1 and CNT2, respectively. The effective output signal must be read when the pre-charge signal is low (PRE=0).

The final block acts as an inverter (Figure 4).

When PRE is high, CNT12 is turned on, letting VDDL pass through CNT17 and CNT16, that are always on. Thus, the output node is pre-charged to VDDL.

When PRE is low, CNT12 is turned off, and CNT15 is turned on. V_{SCNT17} always remains at VDDL, guaranteeing a constant logic level 1 when PRE is high.

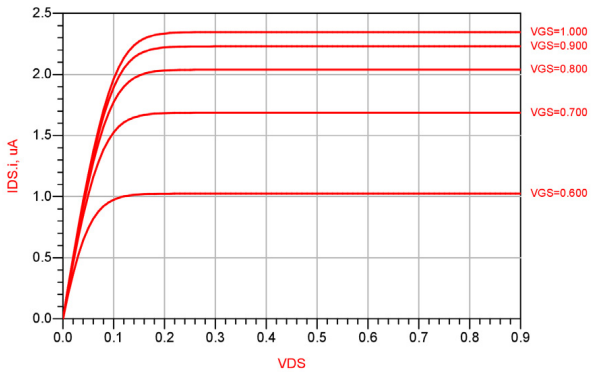

Figure 2. Output I-V characteristics of CNTFET under test.

The parameters used in the simulations have the following values:

· Supply Voltage = 0.9 V;
· CNTFET tube chirality = (15, 2);
· CNTFET Threshold Voltage VTH = 0.3461V;
· CNTFET tube diameter d = 1.26 nm;
· Channel length l = 100 nm;
· Number of sub-bands = 3.

In Figure 5, we reported the simulation of the complex dynamic gate used as a ternary OR (inputs) in Verilog-A, while in Figure 6, the same is shown for PRE and output signals.

Spikes can be seen because of the delay of the different paths of the circuit in the time interval from the pre-charge signal to the evaluation cycle (PRE = 0) [23]. The NAND gate is then designed using the same technique.

In order to verify the NOR gate gain, we have written a MATLAB code to process data from the ADS NOR simulation. It has been simulated the output of this logic gate with a ramp signal input from 0 V to 0.9 V, then deriving it with respect to the input.

Table 1. Truth table of NTI, STI, PTI.

IN	NTI	STI	PTI
0	2	2	2
1	0	1	2
2	0	0	0

Table 2. Truth table of NOR and NAND.

X_a	X_b	NOR	NAND
0	0	2	2
0	1	1	2
0	2	0	2
1	0	1	2
1	1	1	1
1	2	0	1
2	0	0	2
2	1	0	1
2	2	0	0

Table 3. Truth table of a ternary decoder.

SEL	X_0	X_1	X_2
0	2	0	0
1	0	2	0
2	0	0	2

Table 4. Truth table of a ternary Mux.

SEL	OUT
0	I_0
1	I_1
2	I_2

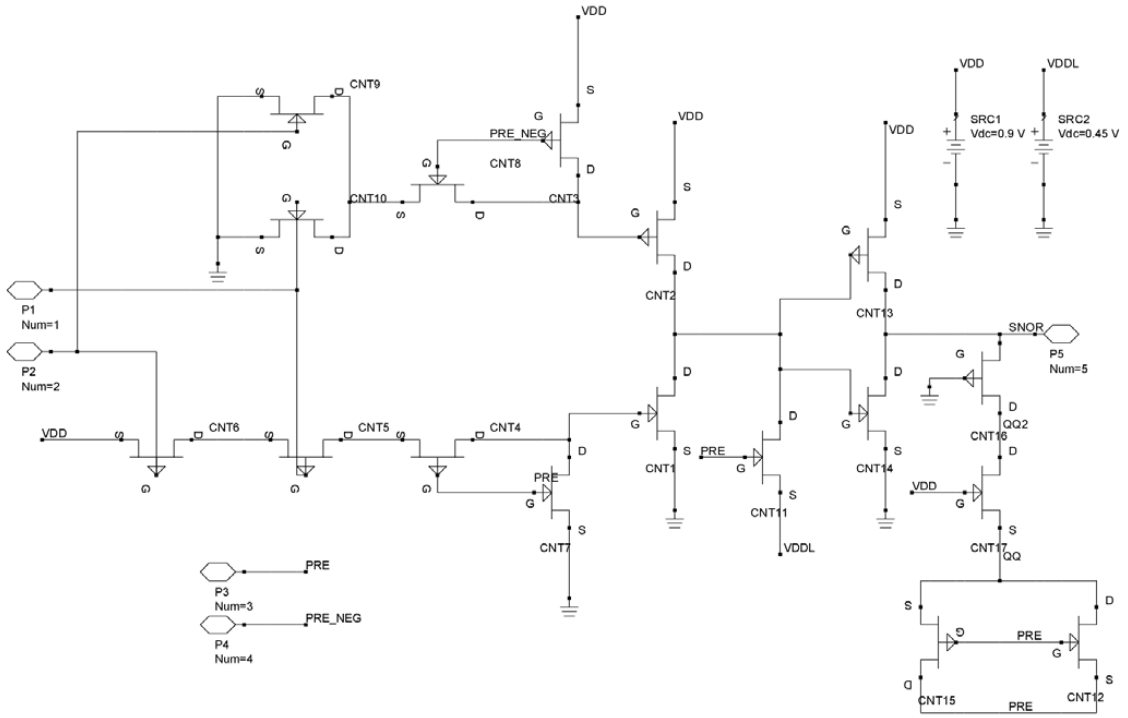

Figure 3. Full schematic of ternary logic NOR.

As we can see from Figure 7, the NOR gate has a gain higher than 5 from 347.5 mV to 369 mV and from 536.5 mV to 558 mV.

With reference to Figure 8, we can compute the propagation time t_p by taking the rise (1->2 & 0->1) and the fall (2->1 & 1->0) time (t_{HL} and t_{LH}, respectively) of the NOR output using the following equation [29]:

$$t_P = \frac{t_{HL} + t_{LH}}{2}$$

The obtained results are reported in Table 5.

4.2. Ternary decoder design

As mentioned, a ternary decoder is a one-input, three-output combinational circuit that generates a response to the input S given by:

$X_i = 2$ if $S = i$

$X_i = 0$ if $S \neq i$

where i could be 0,1, or 2 [29].

As shown in Figure 9, a ternary decoder is composed of 3 inverter gates and 1 NOR gate. U1 is a PTI while U2 and U3 are NTI.

Now, let us consider the truth table of the PTI-NTI series, shown in Table 6.

Since the NTI just inverts the PTI 2 and 0 values, the schematic adopted in this paper is shown in Figure 10.

As shown, it is a PTI followed by a classic inverter, as it will work only with 2 and 0 values.

Parameters used in this simulation are:

· Supply Voltage = 0.9 V;

· CNTFET tube chirality = (12, 2);

· CNTFET Threshold Voltage V_{TH} = 0.4247 V;

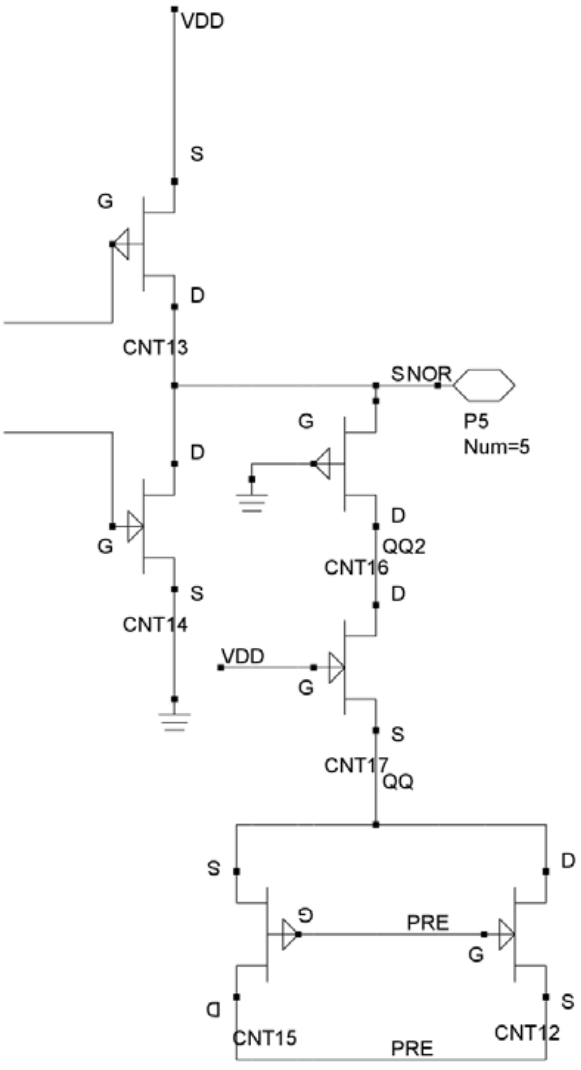

Figure 4. Final block of the ternary logic NOR.

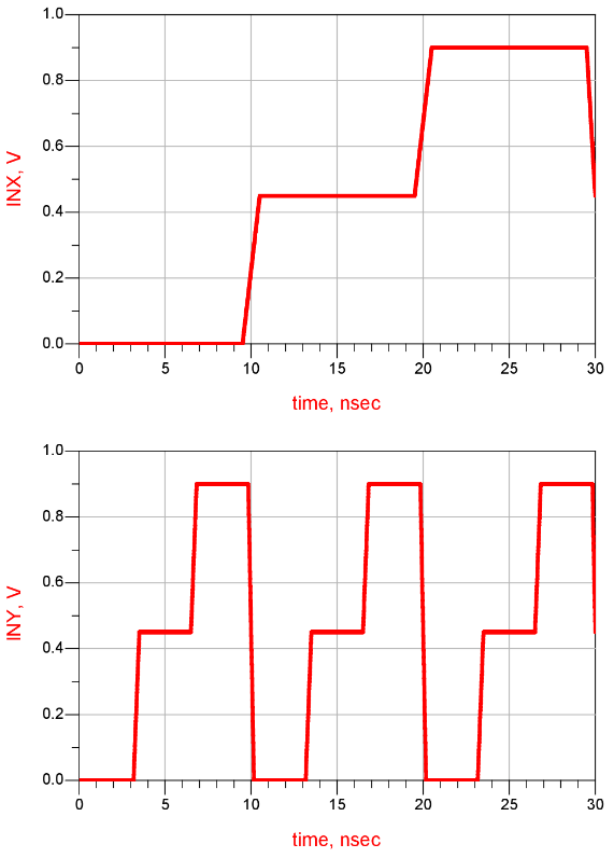

Figure 5. Verilog-A simulation of the complex dynamic gate used as a ternary NOR (inputs).

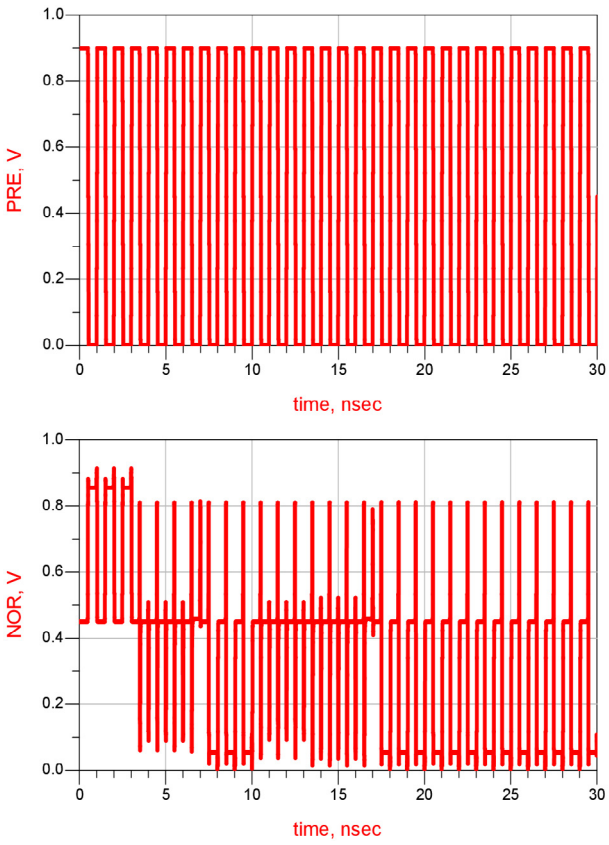

Figure 6. The same of Figure 5 (PRE and output signals).

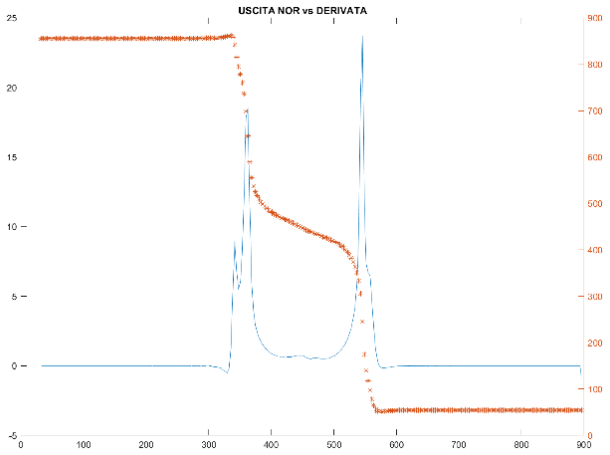

Figure 7. MATLAB simulation showing gain ranges of the complex dynamic gate used as a ternary NOR.

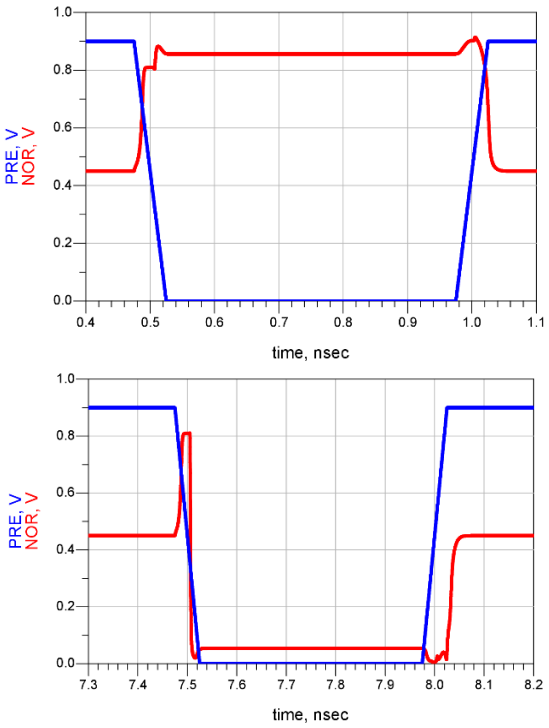

Figure 8. ADS simulation showing rise and fall times.

Table 5. Propagation times.

Delay (ps)	t_R	t_F	t_P
1.2	12.59	25.33	18.96
1.0	45.95	15	30.48

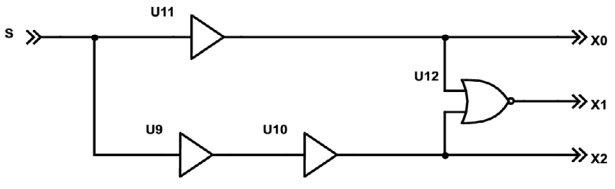

Figure 9. Block diagram of a ternary decoder.

· CNTFET tube diameter d = 1.0267 nm;
· Channel length l = 100 nm;
· Number of sub-bands = 3

In Figure 11, we reported the simulation of the ternary decoder in Verilog-A.

We wish to emphasize that all simulations are obtained using Verilog-A, contrary to the previous designs [23, 25], proposed in the literature, which use SPICE, the most common simulation tool for a designer.

However, in our SPICE simulations, obtained using ABM library as in [5], we have found several problems, among which the main one is:

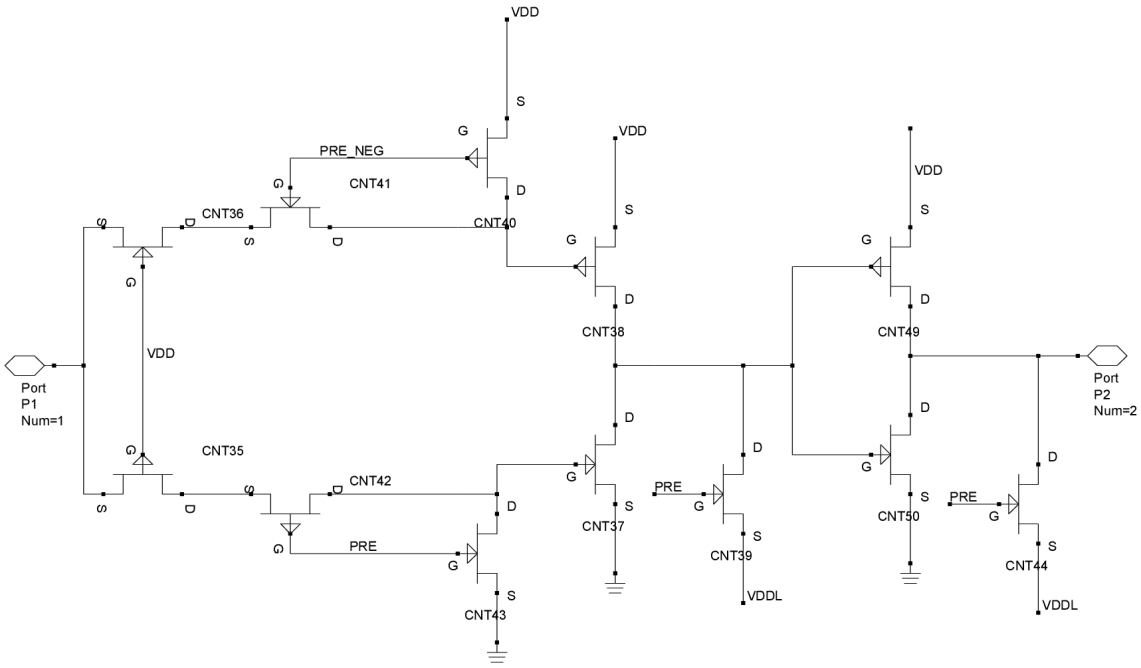

Figure 10. Schematic of the PTI-NTI series.

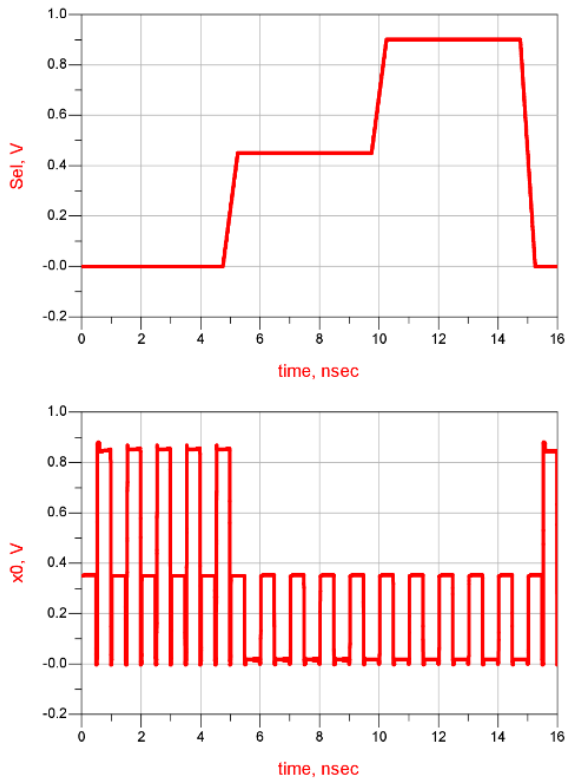

Figure 11. Simulation of ternary decoder in Verilog-A.

Table 6. Truth table of the PTI-NTI series.

IN	PTI	NTI
0	2	0
1	2	0
2	0	2

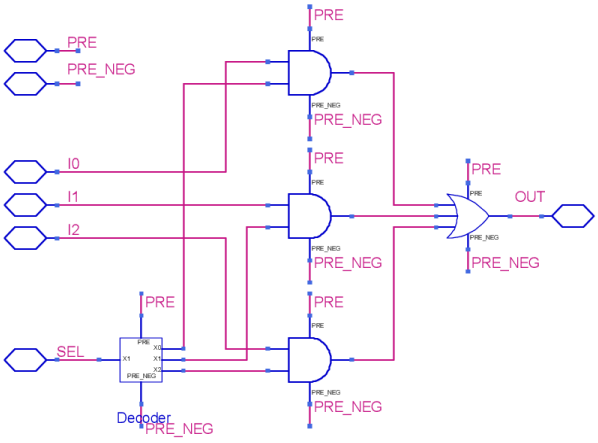

Figure 12. Block diagrams of the ternary 3x1 Mux.

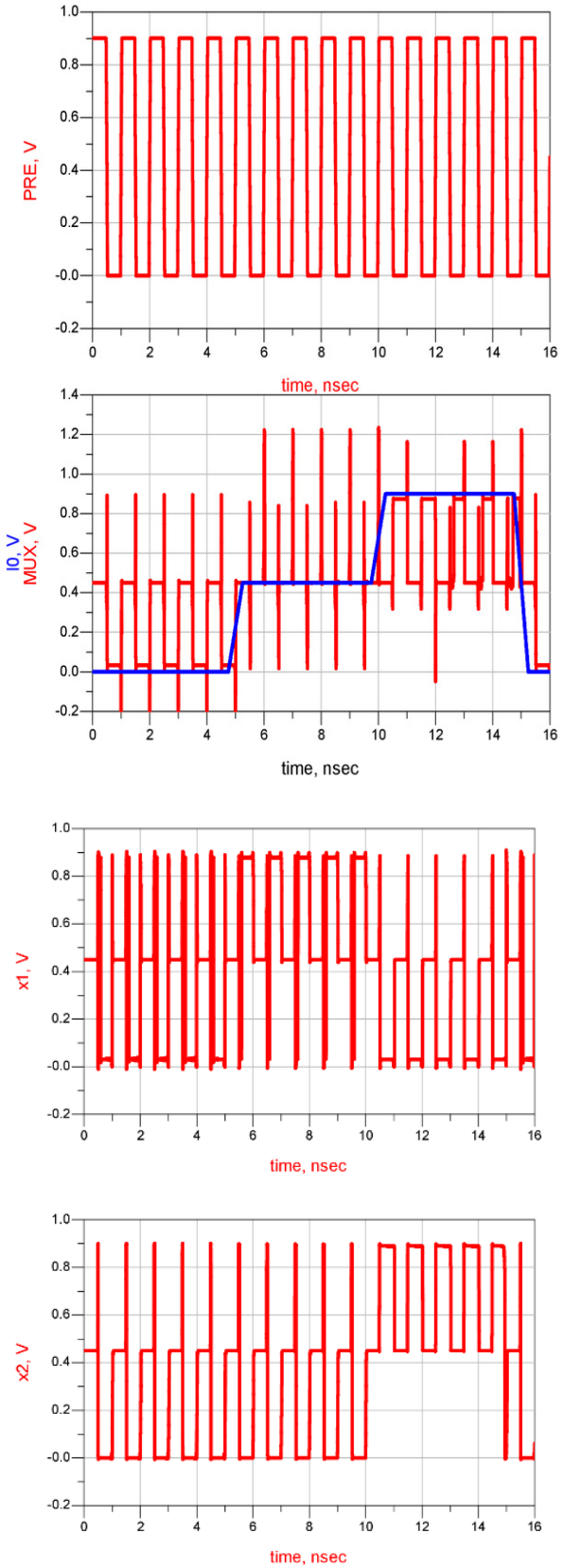

Figure 13. ADS simulation of the ternary Mux.

Any voltage over 10^9 V triggers an overflow error in SPICE, and therefore, all model expressions must be scaled to avoid exceeding this limit in any connection. Similar overflow errors could also happen for the currents,

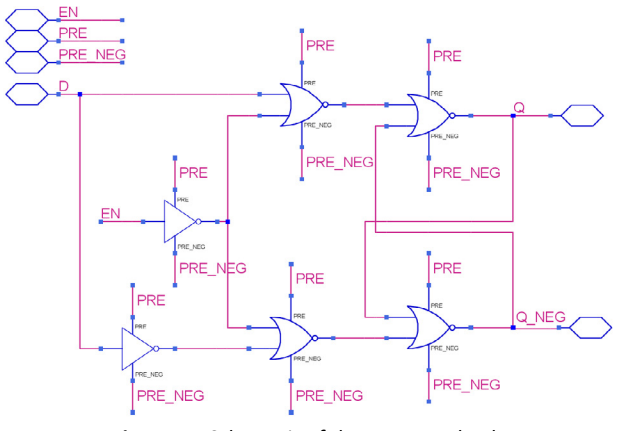

Figure 14. Schematic of the ternary D-latch.

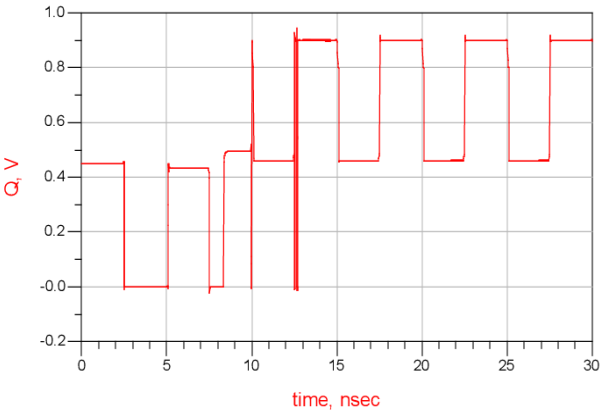

Figure 15. ADS simulation of a ternary D-latch.

but we have avoided this problem, since all utilized model expressions are represented by voltages.

The gate-drain and gate-source capacitances, which depend on bias voltages, can be obtained either as an integral of current or as a derivative of voltage. In the first case, we introduce integration errors because of very small values of currents and time steps, while, in the second case, we introduce noise coming from derivative calculation.

ABM blocks are not simulated exactly. In SPICE, any simple block in the circuit is represented by an equation and, at each time step, the complete system of equations is solved by numerical approximations. This implies that the output of any ABM block is not the exact result of the block operator applied to the input, even for the simplest operators.

The schematic used to simulate the CNTFET model was so large that we decided to use capacitances dependent only on the first band, which is the dominant component of capacitances at low voltages. Nevertheless, when we have used our model [2-3] in the proposed designs, the processing times have been quite high (up to one hour).

Debugging of formulae, expressed as schematics, has been very difficult.

The previous problems have led us to utilize Verilog-A language, which is a part of Verilog-AMS, a high-level description language for Analog and Mixed Signal circuits.

4.3. Ternary 3x1 Mux design

As shown in Table 4, a ternary Mux selects one of its three input signals, delivering the selected input at the output (*3x1* ternary multiplexer). That is, if S = 2, the output will be 0, 1, or 2 if I_2 is 0, 1, or 2, respectively.

As shown in Figure 12, a ternary Mux is composed of a ternary Decoder, a ternary AND gate, and a ternary three-inputs OR gate [13].

In the following circuits, we show the connections for PRE and PRE_NEG, respectively, above and under the logical gates.

In this case, the used parameters are:

· Supply Voltage = 0.9 V;
· CNTFET tube chirality = (13, 0);
· CNTFET Threshold Voltage V_{TH} = 0.43 V;
· CNTFET tube diameter d = 1.02 nm;
· Channel length l = 100 nm;
· Number of sub-bands = 3.

In Figure 13, we reported the relative ADS simulation.

The upper part of Figure 13 shows the PRE signal, while in the lower part, we show in blue the input signal and in red the output signal. Only when the PRE signal is low, the output is valid, and it is evident that the output, during the valid phase of PRE, presents the levels of input port I0, I1, and I2 (which have been set respectively to 0, 1, and 2) as the input signal changes its values from 0 to 1 to 2.

4.4. Ternary D-latch design

A ternary D-latch is built like a binary flip-flop. It clearly delivers three logic levels, and it is called flip-flop as a result. The ternary D-latch circuit implemented in this paper is reported in Figure 14.

We presented this circuit as a test of the logic design of an elementary gate. A much better result would be possible when the clock is removed from every single gate and used at the circuit level.

For this design, the used parameters have been:

· Supply Voltage = 0.9 V;
· CNTFET tube chirality = (9, 2);
· CNTFET Threshold Voltage V_{TH} = 0.55 V;
· CNTFET tube diameter d = 0.80 nm;
· Channel length l = 100 nm;
· Number of sub-bands = 3.

In Figure 15, we reported the relative ADS simulation.

As shown in Figure 15, the input signal EN enables the circuit only for the first part of the simulation and inhibits it during the second half. The input signal D sweeps from 0 to 2, testing all possible input signal values. Since the output signal Q is valid only when the PRE signal is low, we see that the output follows the D values when the EN is high, changing from 0 to 1 and then to 2, while when EN is low, it holds the last value 2.

Moreover, we note that the Q signal presents a slow transition at 7.5 ns, which is caused by the non-optimized circuit design due to the clock distribution at every single gate. Nonetheless, this circuit shows that the logic values can be held correctly using the CNTFET version of 3-level gates proposed in [25].

5. Conclusions and future developments

In this paper, we show how CNTFETs can be used in the design of ternary logic gates, which are a promising alternative to the conventional binary logic design.

In particular, we presented the design of a ternary NOR gate, a ternary decoder, a ternary MUX, and a ternary D latch using the CNTFET model already proposed by us.

In all proposed designs we have considered a clock signal in order to pre-charge, and to evaluate a node, and in this way, the design does not rely on the precise growth of tubes with different diameters and threshold voltages.

All simulations are obtained using Verilog-A, contrary to the previous designs [23, 25], proposed in the literature, which use SPICE. In fact, the novelty Proposed in this article is the first time a comprehensive Verilog-A-based simulation for ternary logic gates using CNTFETs is proposed.

Although SPICE still has a huge importance in the electronic design, since a great number of commercial devices are described by SPICE models and major chip producers distribute their simulation libraries for SPICE, also in this paper, we had confirmation about our idea that Verilog-A is a useful tool to help circuit designers to devise these very new nascent architectures, although its diffusion is still very limited, and nowadays most of its libraries are dedicated to RF.

The results from ADS simulations are encouraging and show that the dynamic ternary logic gate can be a viable approach for low-power and high-speed design in the CNTFET domain.

Moreover, we intend to repeat the proposed technique considering other logic gates and using also other CNTFET models, proposed in literature, such as the VS-CNFET model [21-22], in order to make further comparisons.

Currently, we are also investigating the effect of noise [30-33] in the CNTFET-based design of analogue and digital circuits.

Moreover, we are studying the impact of technology on CNTFET-based circuits performance [34-35].

Conflicts of interest

The authors declare that they have no conflict of interest.

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