

Sol – Gel Spin Coated Cadmium Sulphide Thin Films on Silicon (1 0 0) Substrates for Optoelectronic Applications

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Abstract

Cadmium chalcogenides with appropriate band gap energy have been attracting a great deal of attention because of their potential applications in optoelectronic devices. In this work CdS thin films were deposited on p – type silicon substrates by sol – gel spin coating method at different substrate temperatures. The CdS deposited wafers were characterized by X-ray diffraction method (XRD), Scanning Electron Microscopy (SEM), Photoluminescence spectroscopy (PL), Raman spectroscopy and Fourier Transform Infra – Red spectroscopy (FTIR). XRD analysis showed that the films have crystallites with classical hexagonal structure along (0 0 2) plane. The grain size was found to be in the range of 111.79 nm to 167.66 nm varying with the annealing temperature. The SEM micrograph of annealed CdS thin film showed uniform granular structures with very well defined grain boundaries all over the surface. The Raman spectra of the CdS films presented a well-resolved line at 300 cm^{-1} (1LO) and at 611 cm^{-1} (2LO). PL spectrum showed a broad peak centered around 2.19 eV (508.5 nm) which can be attributed to the defect/trap related transitions. FTIR analysis showed absorption bands corresponding to Cd and S. The electrical property revealed that the resistivity decreases when the samples were annealed.

Keywords: CdS, Sol - Gel process, Spin coating technique, XRD, PL, Raman, FTIR, Four point probe.

1. INTRODUCTION

CdS, belonging to the II–VI group is one of the promising materials for optoelectronic applications. The deposition of CdS films has become increasingly important in recent years due to the widened industrial application with a large number of uses [1–3]. For example the hetero junctions, based on CdS thin films are very promising structures for solar cells because of suitable band gap, optical absorption and good stability of the used materials [4–7]. CdS does not play a direct role in photovoltaic conversion of solar radiation, however, it is adequate as an optical window and preferred over other materials of wide band gap due to its compact crystallographic cell and

electronic affinity with CuInSe₂, InP, CdTe and other p-type semiconductors [8]. Several methods are reported for the preparation of CdS thin film such as electro deposition, Pulsed laser deposition, Physical vapor deposition, vacuum evaporation and closed space sublimation [9]. Compared to other conventional methods, sol – gel route has received much attention in current decades, owing to its better qualities which include low cost, ease of composition control, good film adherence & homogeneity and reproducibility of uniform films, even at shorter processing time. Moreover sol-gel method permits molecular-level mixing and processing of raw materials and

precursors, at relatively lower temperature [10]. It also does not limit the choice of the substrate material.

The modern electronics world greatly depends on silicon dioxide for the manufacture of semiconductors, wire insulation and fiber optic cables. Crystalline Silicon's physical and chemical properties make it as a versatile material in accomplishing physical, structural and electrical tasks in the fabrication of electronic devices. In view of fabricating p-n heterostructure, we choose p-type silicon as a substrate on which n-type CdS was coated and studied.

In the present work, the spin coating technique has been employed for the deposition of CdS films on silicon substrates, which is simple, relatively easier method and ideal for large area thin film preparation. The effect of annealing on the structural, surface morphological optical and electrical properties of the prepared CdS nanocrystalline films has been studied. The results obtained are discussed and compared.

2. MATERIALS AND METHODS

2.1. Synthesis of CdS Thin Films

In the present study CdS particles have been embedded in polyethylene glycol based solution. Polyethylene glycol (PEG 400, Merck) sol was prepared by mixing 0.6 ml of PEG with 8.9 ml of ethanol and 0.5 ml of acetic acid under stirring for 1 hour. 0.1 M of Cadmium nitrate and Thiourea were used as the precursors for incorporation of Cd and S respectively. These precursors were dissolved in ethanol by stirring. The prepared solution was slowly added to the PEG sol with vigorous stirring for 6 hour to obtain the final sol. The spin-coating technique was used to prepare thin films on to silicon substrates using the above sol. The substrates were rotated at a speed of 1000 rpm for 30 seconds. After deposition, annealing of the sample is required for the removal of solvent, residual organics and film densification. So the films were post-

annealed in air at 200°C. Repeating the same procedure two more CdS thin film samples were prepared by varying the post annealing temperature as 300°C and 400°C.

2.2. Material Characterization

X-ray diffraction (XRD) analysis was performed with a diffracting angle range of 20° to 80°, using a PANalytical XPERT-PRO X-ray diffractometer with Cu K α_1 radiation to determine the phase and purity of the samples. The Debye-Scherrer formula was used to estimate the grain size of the CdS samples. Surface morphology of the CdS samples was recorded using Scanning Electron Microscopy (SEM) (ModelTESCAN VEGA-3 LMU). The Raman spectra of the CdS samples were recorded in a Laser-Raman spectrometer built around a double grating monochromator (SPEX 14018). The Photoluminescence (PL) study was carried out with a xenon lamp as light source and the used excitation wavelength was 320 nm. A Fourier Transform Infrared (FTIR) spectrum was recorded using Perkin-Elmer 1605 FTIR spectrometer. The four point probe method was used to measure the resistivity of the CdS samples.

3. RESULTS AND DISCUSSION

3.1. X – Ray diffraction Analysis

Diffractograms of films produced at different substrate temperatures 200, 300 & 400°C are shown in Figure 1(a), 1(b) & 1(c) respectively. XRD analysis showed that the films have highly oriented crystallites, with classical hexagonal structure, with a preferential orientation along the c – axis, (0 0 2) orientation perpendicular to the substrate plane. Zial Raza Khan et.al, also reported that CdS films coated on (1 0 0) Si wafer prepared via thermal evaporation technique exhibited a hexagonal structure with (0 0 2) as the major plane [11]. In addition a much intense (4 0 0) peak was also obtained at $2\theta=69.2^\circ$ which is due to crystalline Si substrate. The average grain

size was calculated from the Scherrer formula, which involves the width of the X-ray diffraction line [12]:

$$D = \frac{k\lambda}{\beta \cos\theta} \text{ (nm)} \quad (1)$$

where, D is the average crystallite size, k is a constant taken to be 0.94, β is the full width at half maximum (FWHM), θ is the Bragg angle and λ is the wavelength of the X-ray source. The grain size was found to increase with an increasing substrate temperature, which is the same behavior as

that is reported by Ashour et.al, [13].

Thus, the film with the higher post annealing temperature has a better crystalline quality, as indicated from its XRD pattern. Increasing the substrate temperature, decreases the density of the nucleation centers and under these circumstances, a small number of centers start to grow, resulting in larger grains [14]. It is clear that substrate temperature plays an important role in determining the structure of the CdS films.

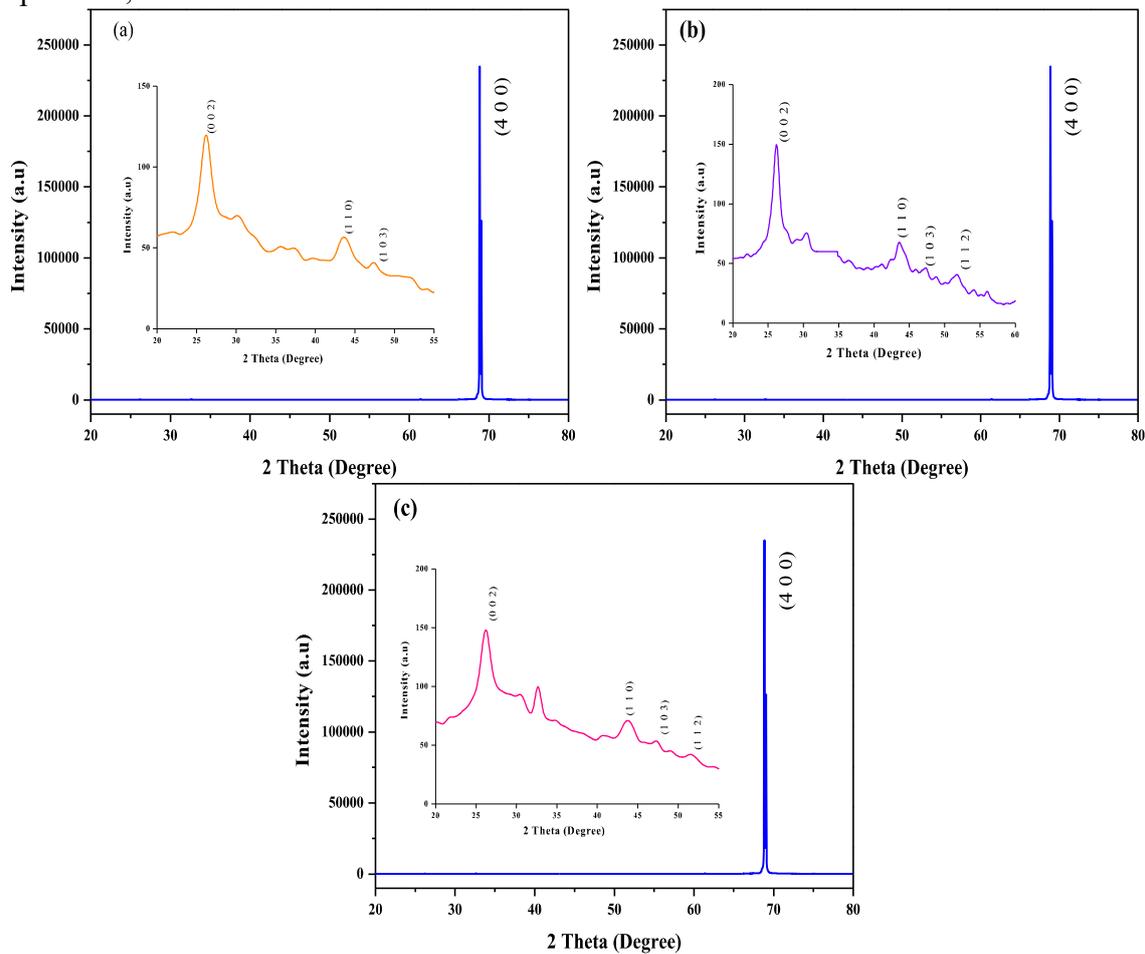


Figure 1. XRD pattern of CdS thin films for different post annealing temperature.

Table 1. XRD data of CdS/Si thin films

Annealing Temperature (°C)	Unit cell Volume V (Å) ³	Lattice Parameter		Crystallite Size D (nm)	Strain $\times 10^{-5}$	Dislocation Density δ ($\times 10^{14}$) (lines/m ²)
		a (Å)	c (Å)			
200	102.50	4.171	6.803	111.79	1.85	0.80
300	104.94	4.224	6.792	139.73	1.48	0.51
400	105.45	4.265	6.694	167.66	1.24	0.36
JCPDS reference	99.45	4.136	6.713	-----	-----	-----

From the XRD data the strain (ϵ), the lattice parameters 'a' & 'c' and the volume of the unit cell were evaluated using the relations, [15],

$$\frac{1}{d^2} = \frac{4}{3} \frac{h^2 + hk + k^2}{a^2} + \frac{l^2}{c^2} \quad (2)$$

$$V = \frac{\sqrt{3}}{2} a^2 c \quad (3)$$

$$\epsilon = \frac{\beta \cos\theta}{4} \quad (4)$$

Where 'd' is the interplanar spacing. The calculated structural parameter values are given in Table 1. The obtained lattice parameters of the CdS films agreed well with the standard JCPDS data [Card No: 06 – 0314].

The dislocation density (δ), defined as the length of dislocation lines per unit volume, was estimated using the formula [16],

$$\delta = \frac{1}{D^2} \quad (5)$$

where 'D' is the average crystallite size and ' δ ' being the measure of amount of defects in a crystal. The smaller values of δ obtained in the present study confirmed the good crystallinity of the CdS films fabricated by employing the spin coating method. The observed values of lattice parameters, strain and dislocation density agree well with the study reported by G.A.Olopade and S.Z.Lahewil et.al, [17, 18].

3.2. Surface Morphological Analysis

The Scanning Electron Microscopy (SEM) was used for topographic analysis of thin film samples. The SEM micrographs of annealed CdS thin films are shown in Figure 2 (a - c).

The surface of the films is found to be uniform and homogeneous. The SEM micrographs of annealed CdS thin film show uniform granular structures with very well defined grain boundaries all over the surface.

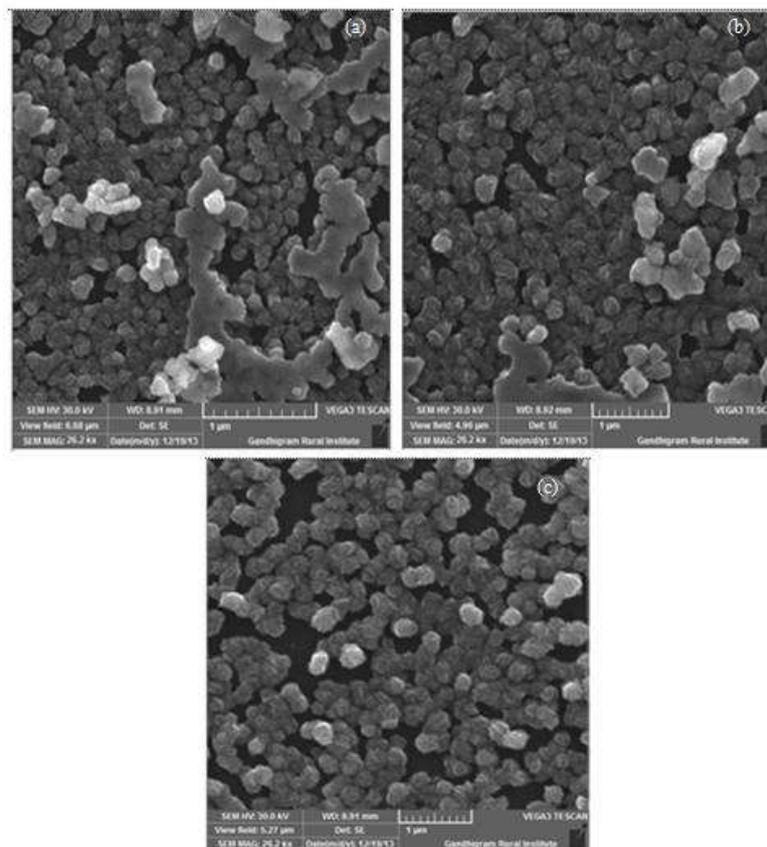


Figure 2 (a - c). SEM micrograph of CdS/Si thin films.

3.3. Raman Spectral Analysis

Raman scattering is very sensitive to the microstructure of nanocrystalline materials and can be used to probe the nanocrystalline CdS thin films. The Raman spectrum of the CdS samples was recorded in a Laser-Raman spectrometer built around a double grating monochromator (SPEX 14018). An argon laser, lasing at 488 nm wavelength with 50mW power was used as the source.

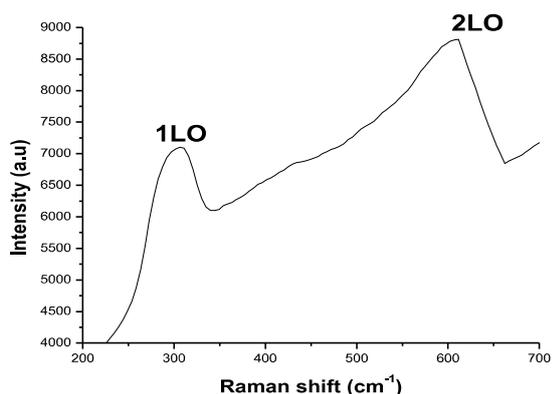


Figure 3. Raman spectra of CdS thin films annealed at 400°C.

Figure 3 shows the Raman spectrum of CdS thin film in which two peaks corresponding to the first and second longitudinal optical phonon modes are present. The well-resolved peak observed at 300 cm^{-1} corresponds to first order scattering of the longitudinal optical (1LO) phonon mode, where the similar 1 LO peak of bulk CdS was observed at 306 cm^{-1} .

This shift is attributed to the effect caused by the grain size [19, 20], i.e. the effect of dimensions on the vibrational properties in small crystalline. The second-order scattering of longitudinal optical (2LO) phonons is also visible at approximately 611 cm^{-1} . The narrow Raman peaks can be attributed to the better crystallinity of CdS film [21]. The peaks at 1LO (300 cm^{-1}) and 2LO (601 cm^{-1}) were also reported by Routkevitch et.al, [22].

3.4. Photoluminescence Analysis

Room temperature photoluminescence (PL) spectra of the nanocrystalline CdS thin film deposited on silicon substrates are

shown in Figure 4. The excitation wavelength for the PL study was 380 nm. The PL spectra show appearance of a broad band extending from 450 to 650 nm. The broad peak centered at around 2.19 eV (508.5 nm) for 200°C annealed sample is attributed to the defect/trap related transitions. The origin of the defects levels may be associated with sulfur vacancies, extrinsic defects or impurities. For 300°C annealed sample, an emission band packing at around 618 nm, called red band is appeared and it is interpreted as the transition of electron trapped at surface states to the valence band.

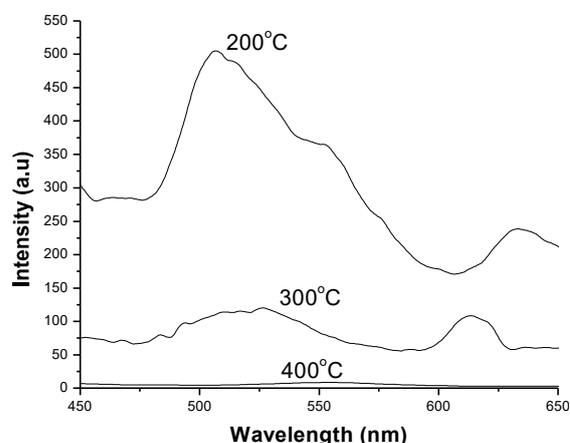


Figure 4. PL spectra of CdS/Si thin films for different annealing temperature.

The appearance of such trap related peaks (sub band gap emissions) in the PL spectra in nanocrystalline CdS were also reported previously [23], although the position of traps varies.

It was also observed, that at higher annealing temperature the crystal growth is better than that at lower annealing temperature i.e., the defect states are reduced at higher annealing temperature. Moreover, the nano CdS/Si samples exhibited remarkably strong band edge related blue shifted luminescence, when the annealing temperature is increased. Similar observations were also reported by Hasselbarth et.al, and they explained the origin of this broad peak was due to the surface recombination taking place in CdS nanoparticles [24].

3.5. FTIR Spectral Analysis

FTIR spectra of CdS nanocrystalline thin films deposited on Si (1 0 0) substrates and annealed at three different temperature are shown in Figure 5.

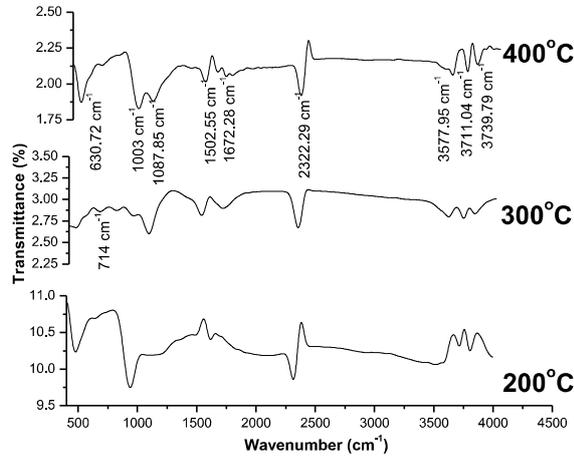


Figure 5. FTIR spectra of CdS/Si thin films for different annealing temperature.

The IR frequencies along with the vibrational assignments for CdS nanocrystalline thin films are given in Table 2.

Table 2. Vibrational assignments of CdS thin film on Si (1 0 0) substrate with positions

Positions (cm ⁻¹)	Assignments
685, 714	Cd – S stretching vibrations
630.72	Cd – S stretching vibrations
1087.85	Si - O stretching vibrations
1502.55, 1672.28	Bending vibrations, H ₂ O
3577.95	O–H stretching vibrations, H ₂ O

The absorption band present at 3577.95 cm⁻¹ is due to the O–H stretching vibrations of water molecules. A weak peak present at 2322.29 cm⁻¹ is due to S–H bond [25]. Presence of SO₂ stretching mode at 1087.85 cm⁻¹ confirms the successful incorporation of the sulfonic group. The vibration absorption peak at 630.72 cm⁻¹ is due to Cd–S stretching. The two medium strong bands at 685 and 714 cm⁻¹ in FTIR spectra of CdS can be assigned to Cd–S stretching [26]. Moreover, the peak in the range of 1105 -

1150 cm⁻¹ is due to the asymmetric stretching vibrations of Si-O-Si bond present in the CdS/Si thin films [27].

3.6. Resistivity (ρ) Measurement Using Four Point Probe

The four point probe method was used to measure the resistivity of the CdS layers. A JADEL of model RM3000 current source was used to pass in the current and measure the voltage drop across the semiconductor. Figure 6 (a - c) presents the voltage – current characteristics of CdS thin films deposited on Si wafer.

A known current was passed in through the outer two probes while the voltage drop was measured using the two inner probes. A graph of voltage against current was plotted to obtain the slope (V/I). Semiconductor resistivity ρ was then computed from the formula

$$\rho = \frac{\rho_0}{G_7 \left(\frac{W}{S} \right)} \quad (6)$$

where,

$$\rho_0 = \frac{V}{I} 2\pi s \quad (7)$$

where ρ - resistivity, the function, G₇(W/S) is a divisor for computing resistivity which depends on the value of W - thickness of the film and S - distance between the probes. The calculated resistivity values for the samples annealed at 200, 300 & 400°C were present in Table 3 and it was in the range of 40.1x10³ – 10.3x10³ Ωcm. The decreasing trend with respect to post annealing temperature in the resistivity may be due to increase in the grain size, decrease in grain boundaries and surface defects states of the samples [28]. This is in accordance with Mathew et.al, [29] who suggested that higher annealing temperatures lead to larger grain size and a smooth surface. These results of resistivity are quite similar to those obtained by Su and Choy [30], Duchemin et.al, [31], Ramadan et.al, [32] and Ashour et.al, [13].

Table 3. Resistivity of CdS nanocrystalline thin film deposited on Si Substrate.

Post annealing Temperature (°C)	Resistivity ($10^3 \Omega \text{cm}$)		
	35°C	50°C	75°C
200	40.1	33.5	24.8
300	36.8	27.8	21.6
400	16.0	14.8	10.3

The resistivity of the samples were also studied by varying the substrate

temperatures as 35, 50 and 75°C while doing V - I characterization measurements. The decrease in resistivity of the films (Figure 7) with increase in substrate temperature indicates the semiconducting nature of the film. Figure 7 shows the effect of both post annealing and substrate temperature on resistivity.

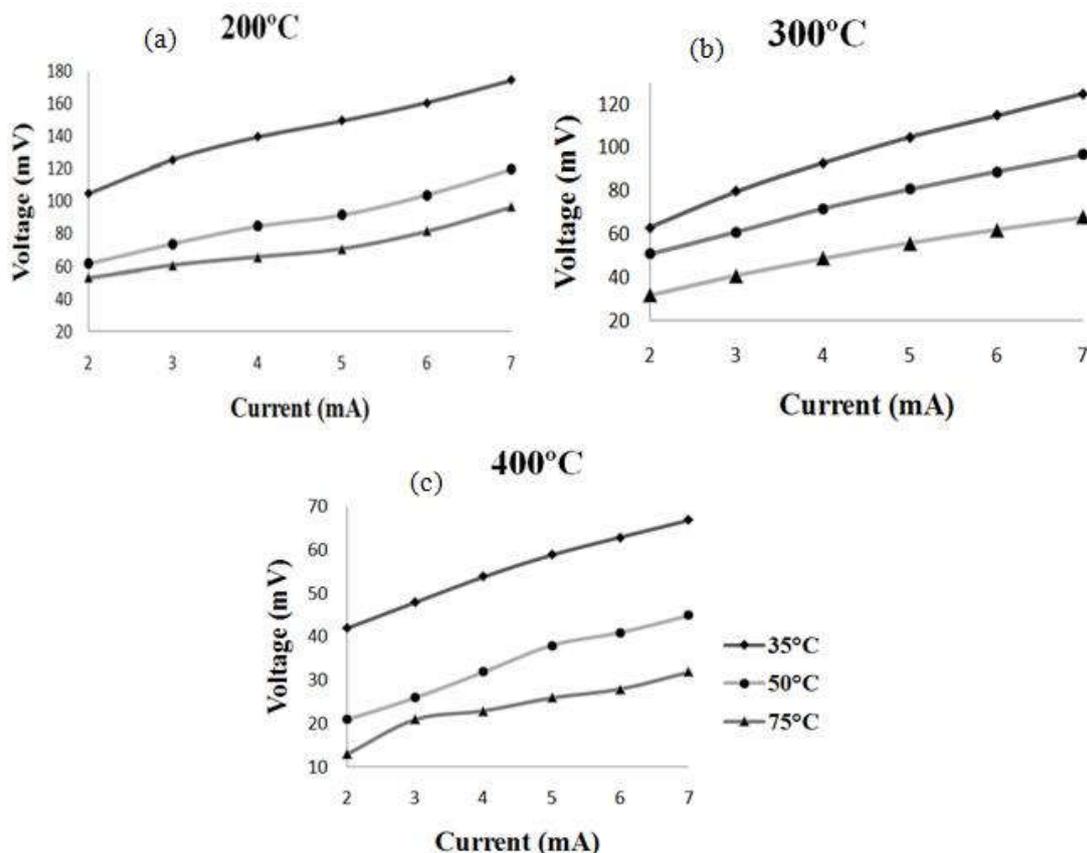


Figure 6. Voltage – Current characteristics of CdS thin films.

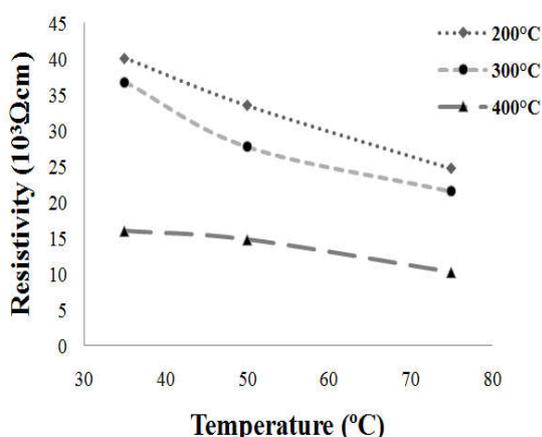


Figure 7. Effect of both post annealing and substrate temperature on resistivity of CdS thin films.

Table 4. Variation of sheet resistance with post annealing temperature

Post annealing Temperature (°C)	Thickness (nm)	Sheet Resistance ($10^9 \Omega$)
200	58.7	6.8
300	55.1	6.7
400	49.9	3.2

Knowing the values of resistivity (ρ) and thickness of thin films (t), the sheet resistance can be determined according to the following relation [33]. The calculated sheet resistance and the thickness of the

CdS/Si films are shown in Table 4 and the corresponding plots are shown in Figure 8.

$$R_s = \frac{\rho}{t} \quad (8)$$

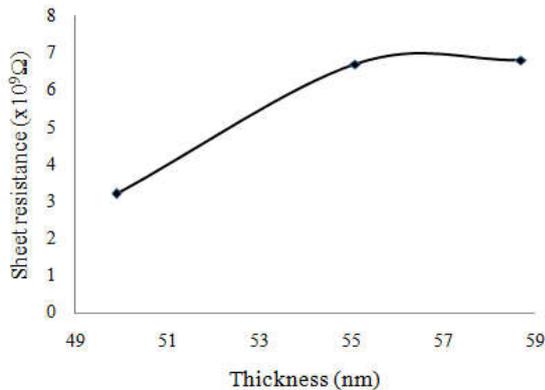


Figure 8. Variation of sheet resistance with thickness of CdS thin film on silicon substrates.

4. CONCLUSIONS

The *n*-type semiconducting thin films of CdS have been deposited by simple and inexpensive sol – gel spin coating

technique on p-type Si (1 0 0) substrates. The effect of annealing on the structural, surface morphological, optical and electrical properties of the prepared films has been studied. The structural studies revealed that the spin coated films have preferential orientation along the (0 0 2) plane with hexagonal structure. Thermal annealing is found to remove the strain present in the CdS films. The Raman spectra showed that the narrowing in the peak has been attributed to an improvement of the crystallinity of CdS. PL spectra showed that the defect states are reduced at higher annealing temperature. FTIR spectrum showed that the characteristic peaks and valleys. The decrease in resistivity values were observed when the samples were annealed. The present study shows that CdS thin films coated on Si substrates proves to be a promising candidate for the fabrication of optoelectronic devices.

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