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Design of Optimized Quantum-dot Cellular Automata RS Flip Flops

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Abstract

Complementary metal-oxide semiconductor (CMOS) technology has been the industry standard to implement Very Large Scale Integrated (VLSI) devices for the last two decades. Due to the consequences of miniaturization of such devices (i.e. increasing switching speeds, increasing complexity and decreasing power consumption), it is essential to replace them with a new technology. Quantum-dot cellular automata (QCA) is one of the alternative technologies proposed as a replacement solution to the fundamental limits of CMOS technology. QCA has the potential to be one of the features promising nanotechnologies because of its higher speed, smaller size and lower power consumption in comparison with transistor-based technology. This work proposes optimized QCA RS (Reset Set) flip flops. The proposed structures are simulated and validated using QCADesigner software. In comparison with the previous works the proposed QCA RS flip flops require the minimum number of cells, area and delay. Also, in comparison with CMOS technology our QCA designs are more efficient in terms of area, delay and frequency. Therefore, these structures can be used to design nanoscale circuits.

Keywords: *Quantum-dot Cellular Automata, Majority Gate, QCADesigner, RS Flip Flop.*

1. INRODUCTION

In the last few decades, scaling in feature size and increase in processing power have been achieved by conventional CMOS technology. Due to basic physical limitations, the conventional VLSI technology faces serious challenging problems in feature size reduction. In contrast, relying on unique properties of the electronic devices at nanoscale sizes, nanotechnology opens new horizons for systems and devices. Among these new devices, Quantum-dot Cellular Automata (QCA) [1, 2] relies on new physical phenomena, and innovative techniques that radically depart from a CMOS-based model. In QCA, the digital information is processed using polarization rather than current. In QCA, binary information is stored as the position of individual electrons (a bi-stable charge configuration) [3]. The fundamental unit of the QCA is the QCA cell. The QCA cell created with four quantum dots (a position, in which a charge can be localized) and two electrons as shown in Fig. 1a [2, 3]. These electrons are free to tunnel between the adjacent quantum dots, but not cells. As shown in Fig. 1a, binary information is encoded in the two possible polarizations (cell polarization P= +1 to represent logic"1" and P=-1 to represent logic"0") [3, 4]. Various types of QCA devices can be constructed using different cell arrangements. The fundamental QCA gates are the three-input majority Gate, wire and inverter. The QCA wire is shown in Fig.1b. In a QCA wire, the binary signal propagates from the input to output because of the electrostatic interactions between the cells. The QCA inverter Gate is shown in Fig.1c.The simplest structure of the inverter Gate is shown in Fig. 1d, which is usually formed by placing the cells with only their corners touching. The QCA majority Gate performs a three input logic function as:

$$f = M(a,b,c) = a.b + a.c + b.c \quad (1)$$

Majority gate can be realized by 5 QCA cells, as shown in Fig. 1e [4]. Logic AND and OR Gates can be implemented using the majority Gate as follow:

$$a.b = M(a,b,0) \quad (2)$$

$$a + b = M(a,b,1) \quad (3)$$

The circuit diagram of the majority Gate is shown in Fig. 1f.

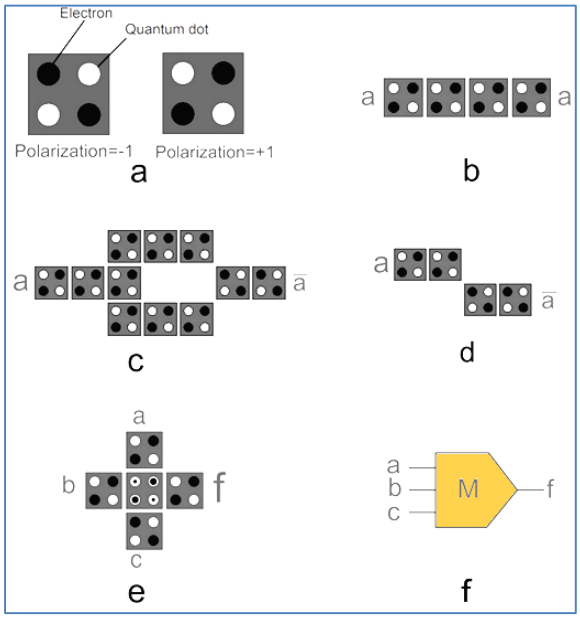

Figure 1*. (a) QCA Cell (b) Binary wire (c) QCA inverters using 11 cells (d) QCA inverters using 4 cells (e) QCA implementation of majority Gate (f) Circuit diagram of majority Gate.*

The circuits in QCA technology require a clock to control and synchronize the information flow and also to provide the power to run the circuit. Unlike CMOS technology, which its clock pulse consists of an upper phase and a lower phase, the QCA clock pulse has four phases: switch, release, hold and rest, which are represented as shown in the Fig. 2. In the switch phase, QCA cell is influenced by its neighbors and its polarization settles down to one of the two ground polarization states. In the hold phase, the cell is latched to its current polarization state. In the release phase, the cell starts to lose its polarization. In the relax phase, the electrons are free to tunnel and delocalize themselves. The QCA cell polarization is determined when it is in the switch phase by the polarization of its neighboring cells, which are at the switch or hold phase.

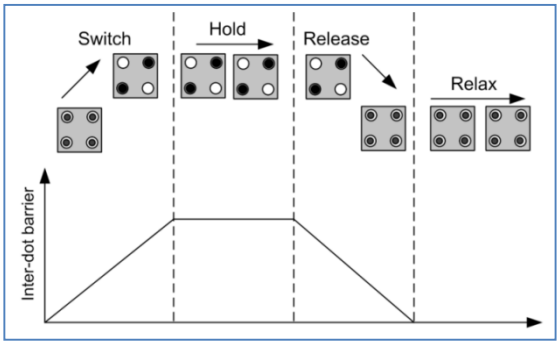

Figure 2. *QCA clocking.*

Using the inverters and majority Gates any QCA circuits including combinational as well as sequential circuits can be implemented [1-9]. In [10], a new low-complexity coplanar 5-input majority gate, which consumes less power compared to prior designs has been introduced. To evaluate the usefulness of this Gate a new one bit full adder circuit has been presented. An efficient design and layout of code converters based on QCA using QCADesigner tool has been introduced in [11]. In [11], a number of new results on binary to gray and gray to binary code converters and detailed simulation using QCADdesigner tool has been presented. A new five input minority gate-based CAM cell has been introduced in [12]. Also, QCADesigner has been used for simulation of the proposed structure and verifying its operation. In [13], an improved full adder with a different formulation for its sum and carry outputs in QCA technology has proposed, which is considerably declined in terms of cell numbers and area, compared to other full adders and delay is kept at minimum. In this paper we proposed optimized QCA RS (Reset Set) flip flops. Two different QCA RS flip flops are presented, which in comparison with the previous works require the minimum number of cells and

less area. Also, they work with less clock phases.

2. RS FLIP FLOP DESIGN

The Boolean expression for an RS flip flop is given by:

$$Q_{n+1} = S + \overline{R}.Q_n \quad (4)$$

The block diagram of the QCA RS flip flop is shown in Fig. 3a [6]. This block diagram is equivalent to the following equation [6]:

$$Q_{n+1} = M(S, \overline{R}, Q_n) \quad (5)$$

Fig.3b shows the first proposed QCA RS flip flop layout. The inner loop of the flip flop has a delay of one clock cycle; therefore at the output, Q is available 5 clocking zones after R and S have been applied. Fig.4 shows the second proposed RF flip flop. In this layout, the inner loop of the flip flop has a delay of one clock cycle; but at the output, Q is available 4 clocking zones after R and S have been applied.

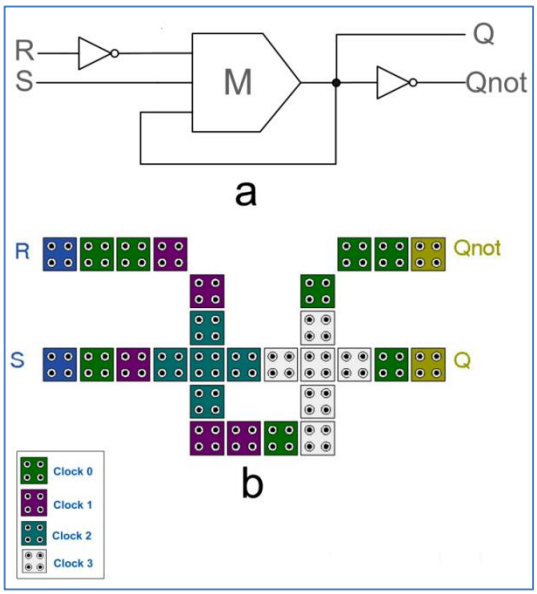

Figure 3. *The first proposed QCA RS flip flop (a): Schematic diagram (b) QCA layout.*

The proposed structure in Fig. 3b is verified using QCADesigner ver.2.0.3 [14], with the following parameters for a bistable approximation [14]: Cell size=18nm, Number of samples=20000, Radius of effect=90nm, Relative permittivity=12.9, Convergence tolerance=0.001, Clock high=9.8e-22J, Clock low=3.8e-23J, Clock amplitude factor =2, Layer separation=11.5nm and Maximum Iterations per sample =100.

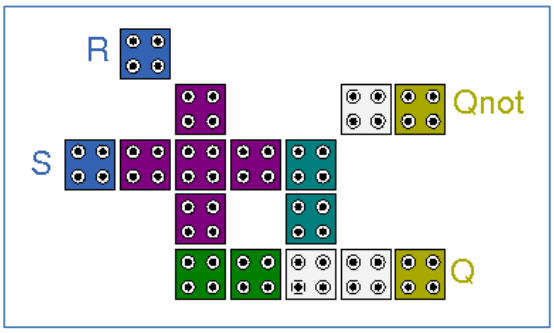

Figure 4. *Layout of the second proposed QCA RS flip flop.*

3. RESULTS AND DISCUSSIONS

Fig.5 and Fig.6 show the fault free simulation results for the proposed QCA RS flip flops. The second proposed structure (Fig.4) is verified using QCADesigner ver.2.0.3 [14], with the following parameters used for a bistable approximation: Cell size=18 nm, Number of samples=12800, Radius of effect=65nm, Relative permittivity=12.9, Convergence tolerance=0.00001, Clock high=9.8e-22J, Clock low=3.8e-23J, Clock amplitude factor =2, Layer separation=11.5nm and Maximum Iterations per sample =1000. Table 1 compares the proposed RS flip flops with the previous works presented in [6, 15-17]. As it is seen from Table 1, in comparison with the previous work presented in [6] the optimization rate (OT) (sometime called "Percentage Reduction") for the first proposed design is 70 % and 60 % in the area and cell count, respectively. Also it is faster. The OT is obtained using the following equation:

$$OT = \left|1 - \frac{X}{Y}\right| * 100 \quad (5)$$

Where X and Y stand for the measured objects (area or cell count) for our designs and the previous designs, respectively. In comparison with the previous work

presented in [6], the second proposed design is faster and the OT is 83 % and 75 % in the area and cell count respectively. Also the second proposed design in comparison with the first proposed design is faster and reduces the area and cell count by 45 % and 38 %, respectively. Therefore, this structure is the best proposed design. In comparison with the best previous QCA RS flip flop presented in [17], the OT for the best proposed design (the second proposed design) is 67% and 51 % in the area and cell count, respectively. Also our design is faster. From these result it is clear that in comparison with the previous works our designs are more efficient in term of cell count, area and delay.

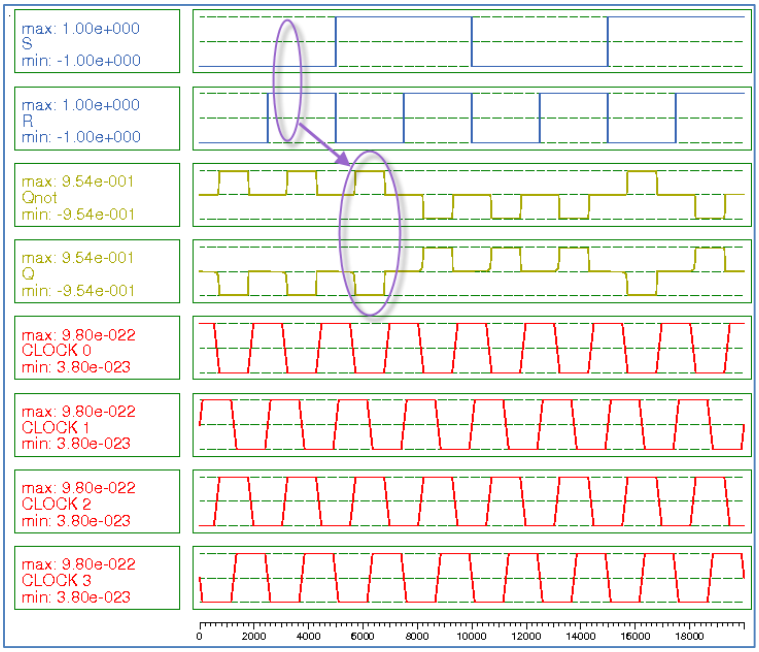

Figure 5. *Simulation result of the first proposed QCA RS Flip-flop (Fault-free Case).*

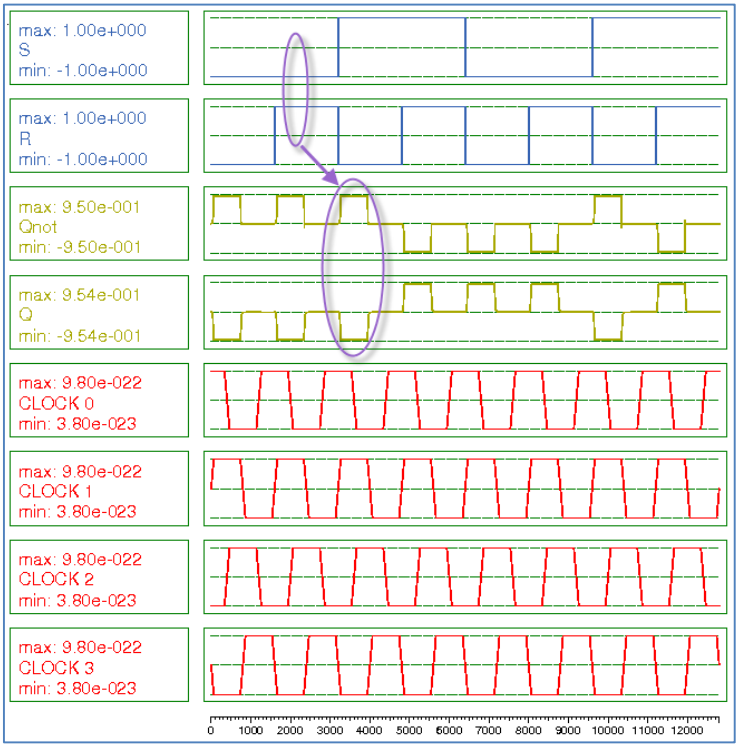

Figure 6. *Simulation result of the second proposed QCA RS Flip-flop (Fault-free Case).*

Table 1. *Comparison between QCA RS Flip Flops.*

References	Area (μm^2)	Cell count	Delay (clock phase)
Ref. [6]	**0.08**	**66**	**7**
Ref. [15]	0.07	60	6
Ref. [16]	0.09	76	6
Ref. [17]	0.04	33	5
The first proposed design	0.024	26	5
The second proposed design	**0.013**	**16**	**4**

Also, we have compared our QCA designs with conventional CMOS technology. Fig. 7 shows the layout of a RS flip flop implemented with 90 nm CMOS technology. The layout shown in Figure 7 has the approximate area equal to 9.65 μm^2. In comparison with this CMOS design, the required areas for our QCA design shown in Fig.3 is about 742 times smaller. Table 2 shows the comparison between the proposed QCA designs and the CMOS work. As shown in Table 2, the proposed QCA RS flip flop in Figure 3 has around 742 times, 174 times, 2750000000 times and 456.8 times improvements in terms of area, delay, power and frequency, respectively.

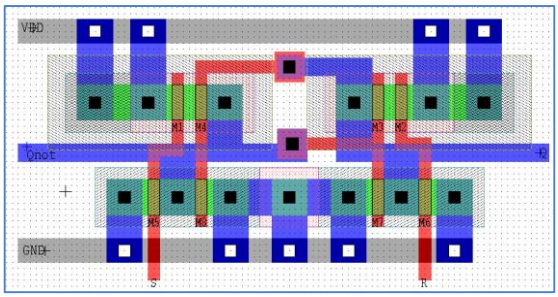

Figure 7. *Layout of a CMOS RSFF.*

Table 2. *Comparison with CMOS Technology.*

Comparison	RS flip flop Designs	
	Fig.7	**Fig.3**
Approximated area (μm^2)	9.65	**0.013**
Delay (ps)	122	**0.700**
Power (μW)	55	2×10^{-8}
Frequency (GHz)	1.25	**571**

4. CONCLUSION

In this paper, we proposed optimized QCA RS flip flops. The proposed structures are validated using the QCADesigner software. In comparison with the previous works, the results showed that these QCA RS flip flops are better in terms of area, cell count and delay. In comparison with the best previous design the best our design reduced the area and cell count by 67% and 51 %, respectively. Therefore, we can use these structures to design nanoscale circuits.

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