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# A Simulation Study of Temperature Variation Effects on I-V Characteristics of CNTFET

**Roberto Marani[1] and Anna Gina Perri[2,*]**

[1]Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy
[2]Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
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***Abstract***

*In this paper we present a simulation study of temperature variation effects on I-V characteristics in Carbon Nanotube Field Effect Transistor. The study is carried out considering different CNTFET models proposed in the literature in order to identify the one more easily implementable in simulation software for electronic circuit design. At first we consider a compact, semi-empirical model, already proposed by us, performing I-V characteristic simulations at different temperatures. Our results are compared with those obtained with two other models: the numerical FETToy model and the Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET), obtaining I-V characteristics comparable with those of two examined models, but with CPU calculation times much lower.*

***Keywords:*** *CNTFET, Modelling, Device Simulation, I-V Characteristics, Temperature Effects, Verilog-A, Computer Aided Design.*

## 1. INRODUCTION

Today the scaling operation of silicon devices is saturated since these devices cannot be more shrunk without degrading their performances for the arising of some phenomena like tunnel effects [1] or the perforation of the gate oxide also for voltages relatively low.

The previous problems can be overcome by resorting to other new devices, such as Carbon NanoTube Field Effect Transistors (CNTFETs), in which, as it is known, the channel is formed by Carbon NanoTubes (CNTs) instead of silicon [1-13].

In literature various CNTFETs models have been proposed, many of which are numerical and make use of self-consistency and therefore they do not allow an easy implementation in circuit simulators (SPICE, Verilog-A or VHDL-AMS), which instead must be the main characteristic in the field of Computer Aided Design (CAD).

In [2-17] we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A. Then our model has been implemented to carry out static and dynamic analysis of analogue and digital circuits [18-19], obtaining a significant improvement compared to Wong model [20-22].

In this paper, we present a simulation study of temperature variation effects on I-V characteristics in Carbon Nanotube Field Effect Transistor. The study is carried out considering different CNTFET models proposed in the literature in order to identify the one more easily implementable in simulation software for electronic circuit design (CAD).

In particular we consider our model performing I-V characteristic simulations at different temperatures. Then we have translated it in the programming language

Verilog [23] and then implemented on the simulator Advanced Design System (ADS).

Our results are compared with those obtained with two other models considered: the numerical model, online available, proposed by NanoHub in FETToy tool [24] and the last Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET), using for this model the version downloadable on website of Stanford University, which refers to Wong model published in [25-26], obtaining I-V characteristics comparable but with a significant improvement, because we have a shorter execution time.

The presentation is organized as follows. Section 2 gives a brief description of the examined DC models, with reference to Equations on which the CNTFET models are based. The discussion of obtained results, together with the description of the setup-work used during the simulations, is given in Section 3. The conclusions and future developments are given in Section 4.

## 2. A BRIEF REVIEW OF THE EXAMINED DC MODELS

An exhaustive description of our CNTFET model is in [2-3]. Therefore we suggest the reader to consult these References.

It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact the most complex part of the model is contained in Verilog A [23]. In particular, the simulation have been run using Advanced Design System (ADS) which is also accept devices described by model written in Verilog A. We have considered a single wall n-CNTFET in the ballistic transport hypothesis. This assumption allowed to define an analytical formula for CNT current.

When a positive voltage $V_{GS}$ is applied between gate-source, the conduction band at the channel beginning decreases by $qV_{CNT}$, where q is the electron charge and $V_{CNT}$ is the surface potential.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [27]:

$$I_{DS} = \frac{4qkT}{h} \sum_{p} \left[ \ln\left(1 + \exp \xi_{Sp}\right) - \ln\left(1 + \exp \xi_{Dp}\right) \right] \quad (1)$$

where *q* is the electron charge, k is the Boltzmann constant, *T* is the absolute temperature, h is the Planck constant, p is the number of sub-bands.

$\xi_{Sp}$ and $\xi_{Dp}$ have the following expressions [2-3]:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT}$$

and (2)

$$\xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT}$$

being $E_{Cp}$ the sub-bands conduction minima, $V_{DS}$ the drain-source voltage and $V_{CNT}$ the surface potential.

In [2] we have proposed, to evaluate $V_{CNT}$, the following approximation:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \dfrac{E_C}{q} \\ V_{GS} - \alpha\left( V_{GS} - \dfrac{E_C}{q} \right) & \text{for } V_{GS} \geq \dfrac{E_C}{q} \end{cases} \quad (3)$$

where $E_C$ is the conduction band minimum for the first sub-band and $\alpha$ is a parameter depending on $V_{DS}$ voltage, CNTFET diameter and gate oxide capacitance $C_{ox}$ [2-3].

Moreover the proposed analytical modelling equations describing the current transport in CNTFETs have been developed from physical electronics [28-29].

In the following simulations our model has been translated in the programming language Verilog-A and then implemented on the simulator Advanced Design System (ADS).

The model implemented in FETToy [24] is a purely numerical model. It is based on the non-equilibrium Green's function (NEGF) formalism, which solves the Schrödinger and Poisson equations under non-equilibrium conditions. The band structure of CNT has been calculated by the tight-binding method [30]. In particular FETToy simulator consists of a set of Matlab scripts that calculate the ballistic I-V characteristics for a conventional MOSFETs, Nanowire MOSFETs and Carbon NanoTube MOSFETs. Only the lowest subband is considered, but it is readily modifiable to include multiple subbands.
The underlying theory is described in detail in [30].

Finally, the Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET) [21-22], named also *Wong model*, is a semi-empirical model that describes the current-voltage (I-V) and capacitance-voltage (C-V) characteristics in a short-channel metal-oxide-semiconductor field-effect transistor (MOSFET) with carbon nanotubes as the channel material.

The key difference between the previous Stanford CNFET model (S-CNFET) [25-26] and the VS-CNFET model [21-22] is the modelling of carrier transport. In particular the VS-CNFET model is based on the semi-empirical virtual source concept calibrated to experimental data. The intrinsic drain current and terminal charges are based on the virtual source (VS) model, with the virtual source velocity extracted from experimental data for different channel lengths (ranging from 3-um down to 15-nm).
Moreover, the VS-CNFET model takes to account the following parasitic effects:

1. Direct source-to-drain and band-to-band tunnelling current calibrated by numerical simulations;
2. Metal-to-CNT contact resistances calibrated by experimental data;
3. Parasitic capacitance including gate-to-CNT fringe capacitances and gate-to-contact coupling capacitances.

The inputs to the VS-CNFET model are the physical device design including device dimensions, CNT diameter, gate oxide thickness, etc.

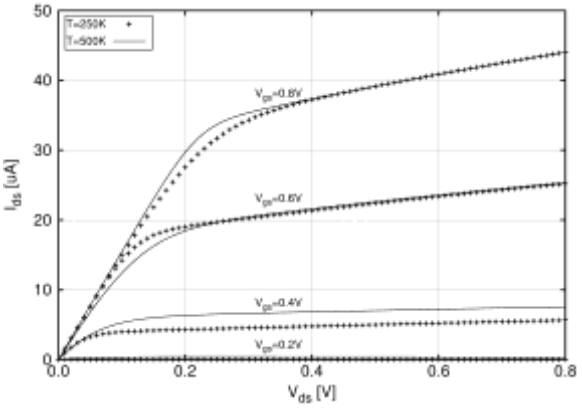
## 3. DISCUSSION OF SIMULATION RESULTS

We referred to the CNTFET features reported in [31] to perform simulations with models described above.

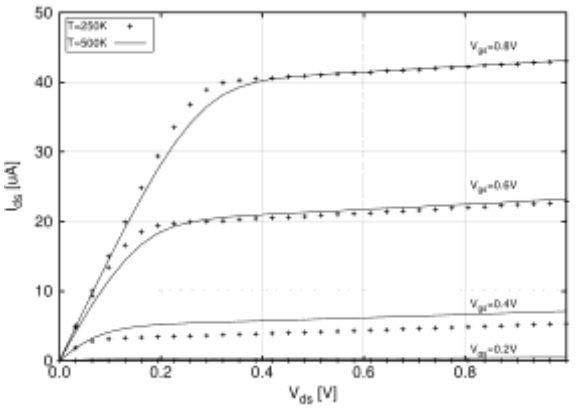
The device has a zig-zag (19,0) CNT structure with approximately 1.5 nm radius which is embedded in cylindrical gate insulator of $HfO_2$ with the thickness and dielectric constant (k) of 2 nm and 16, respectively. The length of source and drain regions is equal to 20 nm. The channel is intrinsic and its length is 20 nm. There is no overlap between the source (drain) and gate regions.

The simulations are performed at the temperature of 250 K and 500 K in Agilent Technologies CAD ambient, Advanced Design System (ADS). In order to simulate with ADS, it has been necessary to develop a new component of the Design Kit, which was added to the model, written in Verilog language.

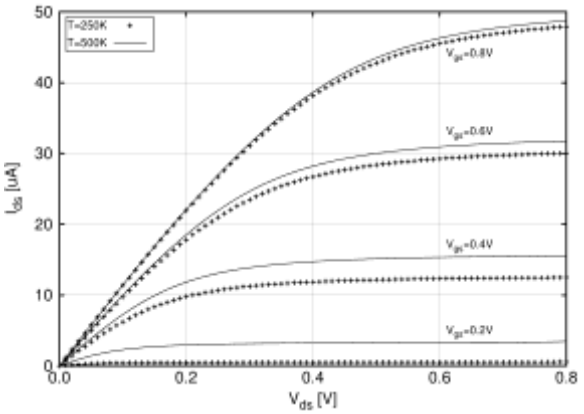
Figure 1 shows the I-V output characteristics of the three considered models, at various temperatures.



(a)




(b)



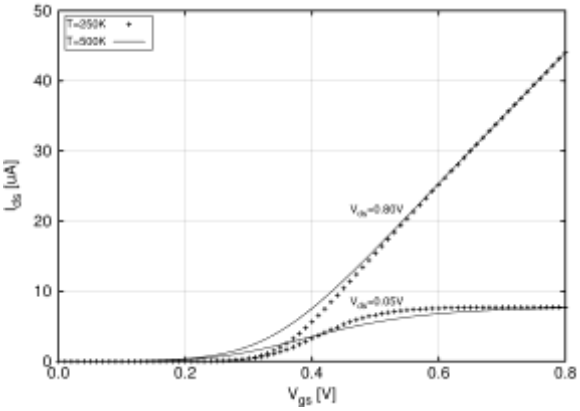

(c)

***Figure 1.*** *$I_{DS}$ versus $V_{DS}$ at different temperatures and different $V_{GS}$ for: our model (a); FETToy model (b); and VS-CNFET model (c).*

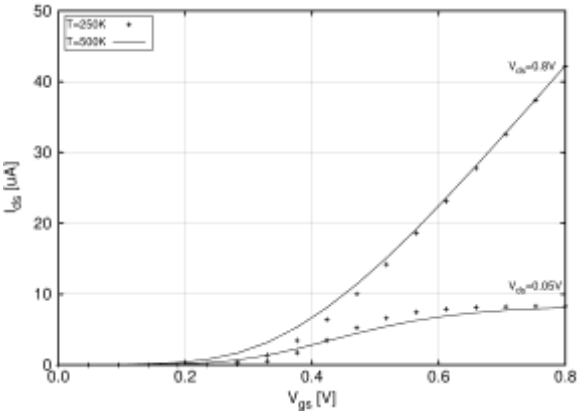
It can be observed from Figure 1 that for low gate source voltages, at temperature of 500 K, the drain current $I_{DS}$ is higher than that at 250 K. In spite of this, as $V_{GS}$ increases at low drain source voltages, $I_{DS}$ at 500 K is less than that at 250 K. As it is possible to note from Fig. 1 (c), it is not verified for the VS-CNFET model.

In the saturation region, by increasing $V_{GS}$, the drain current difference between high and low temperature reduces. It is evident from Figures 1 (a-c) that the drain current in the saturation region and $V_{GS}$ = 0.8 V for 250 K and 500 K are approximately equal. This claim appears to be less verified for model VS-CNFET (Figure 1 (c)) and for the FETToy model for $V_{GS}$ = 0.6 V (Figure 1 (b)).

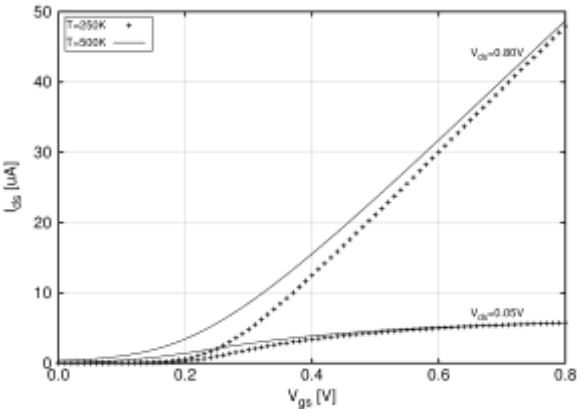
Similarly, Figure 2 shows the trans-characteristics of the device, obtained by the considered three models.




(a)




(b)




(c)

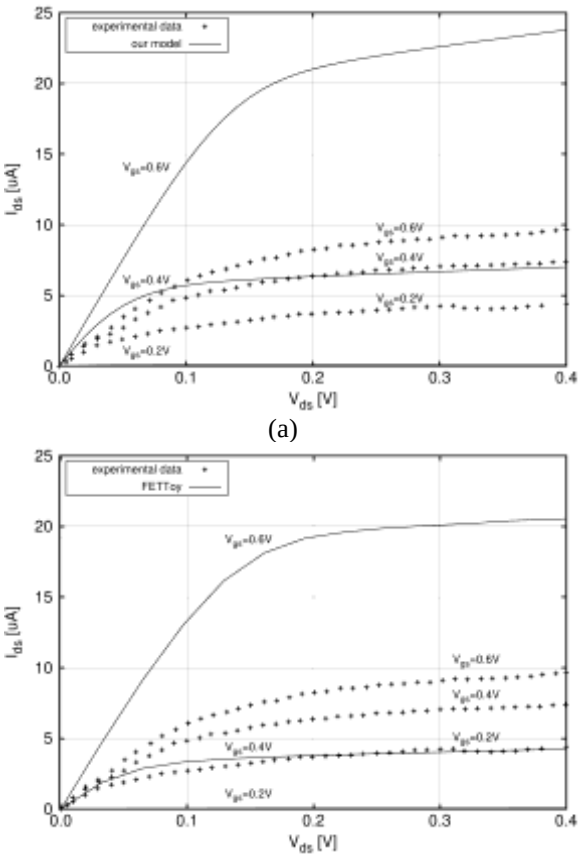
***Figure 2.*** *$I_{DS}$ versus $V_{GS}$ at different temperatures and different $V_{DS}$ for: our model (a); FETToy model (b); and VS-CNFET model (c).*

As it is possible to observe from Figure 2, at $V_{DS}$ = 0.8 V the current raises, when temperature decreases from 500 K to 250

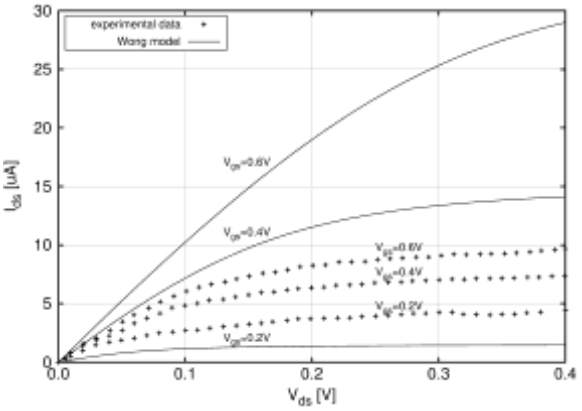
K, while the threshold voltage of the device decreases. Moreover, for $V_{DS}$ > 0.8 V. both in our model and in FETToy model the current dependence on temperature is almost zero, while it is still present in VS-CNFET model. While the current rises with temperature T is present also at $V_{DS}$ = 0.05 V for $V_{GS}$ < 0.4 V, the dependence is inverted for our and FETToy models for $V_{GS}$ > 0.4 V. Instead, in Wong model, the current is almost independent of T for $V_{DS}$ = 0.05 V and $V_{GS}$ > 0.4 V, similarly to what observed in Fig. 1 in the linear region.

Moreover, to validate the obtained data, we have compared the three considered models at 300 K with experimental data [32], as shown in Figure 3.

From Figure 3 we observe that there is a low agreement between experimental values (dots) and those simulated (line) for all three considered models, since, to have low computational cost, they do not consider both ballistic and non-ballistic transport effects [32].




(b)




(c)

***Figure 3.*** *$I_{DS}$ versus $V_{DS}$ at 300 K and different $V_{GS}$ for: our model (a); FETToy model (b); and VS-CNFET model (c); in comparison with experimental data (dots).*

The simulation results at 250 K and 500 K are summarized in Table 1.

In particular we have reported $V_{DS}$ and $I_{DS}$ values in the knee region at different temperature and for different $V_{GS}$. The values of the threshold current are shown in the right part of the Table 1 for the two considered temperatures (250 K and 500 K) and for different gate-source voltages.

From Table 1**,** it is possible to notice, easily, that when $V_{GS}$ increases, the saturation voltage ($V_{DS,SAT}$) increases. This consideration is valid for all models and occurs for the considered temperatures during the simulations.

The results presented show that the values of saturation current for different temperature are equal for high $V_{GS}$ for the proposed model and the FETToy numeric model. Instead Wong model shows a mismatch that increases at low $V_{GS}$ values.

In Table 2**,** we have reported the results extracted from trans-characteristics of Figure 2.

***Table 1.*** *Values of $I_{DS}$ vs $V_{DS}$ at different temperatures for our model (a), FETToy model (b)) and VS-CNFET model (c).*

| $V_{GS}$ | **Knee Region** | | **Saturation Region** (at $V_{DS}$ = 0.8 V) | |
|---|---|---|---|---|
| | 250 K | 500 K | 250 K | 500 K |
| 0.2 V | $V_{DS}$ = 0.027 V<br>$I_{DS}$ = 9.41 nA | $V_{DS}$ = 0.054 V<br>$I_{DS}$ = 288 nA | $I_{DS}$ = 10.5 nA | $I_{DS}$ = 0.365 µA |
| 0.4 V | $V_{DS}$ = 0.043 V<br>$I_{DS}$ = 3.03 µA | $V_{DS}$ = 0.079 V<br>$I_{DS}$ = 4.73 µA | $I_{DS}$ = 5.64 µA | $I_{DS}$ = 7.56 µA |
| 0.6 V | $V_{DS}$ = 0.123 V<br>$I_{DS}$ = 16.3 µA | $V_{DS}$ = 0.146 V<br>$I_{DS}$ = 16.0 µA | $I_{DS}$ = 25.2 µA | $I_{DS}$ = 25.4 µA |
| 0.8 V | $V_{DS}$ = 0.238 V<br>$I_{DS}$ = 30.9 µA | $V_{DS}$ = 0.223 V<br>$I_{DS}$ = 32.0 µA | $I_{DS}$ = 44.1 µA | $I_{DS}$ = 44.1 µA |

(a)

| $V_{GS}$ | **Knee Region** | | **Saturation Region** (at $V_{DS}$ = 0.8 V) | |
|---|---|---|---|---|
| | 250 K | 500 K | 250 K | 500 K |
| 0.2 V | $V_{DS}$ = 0.037 V<br>$I_{DS}$ = 3.6 nA | $V_{DS}$ = 0.059 V<br>$I_{DS}$ = 174 nA | $I_{DS}$ = 154 nA | $I_{DS}$ = 0.416 µA |
| 0.4 V | $V_{DS}$ = 0.051 V<br>$I_{DS}$ = 2.49 µA | $V_{DS}$ = 0.090 V<br>$I_{DS}$ = 3.96 µA | $I_{DS}$ = 4.84 µA | $I_{DS}$ = 6.66 µA |
| 0.6 V | $V_{DS}$ = 0.136 V<br>$I_{DS}$ = 17.2 µA | $V_{DS}$ = 0.166 V<br>$I_{DS}$ = 17.0 µA | $I_{DS}$ = 22.0 µA | $I_{DS}$ = 22.5 µA |
| 0.8 V | $V_{DS}$ = 0.261 V<br>$I_{DS}$ = 37.1 µA | $V_{DS}$ = 0.277 V<br>$I_{DS}$ = 35.6 µA | $I_{DS}$ = 42.2 µA | $I_{DS}$ = 42.3 µA |

(b)

| $V_{GS}$ | **Knee Region** | | **Saturation Region** (at $V_{DS}$ = 0.8 V) | |
|---|---|---|---|---|
| | 250 K | 500 K | 250 K | 500 K |
| 0.2 V | $V_{DS}$ = 0.037 V<br>$I_{DS}$ = 3.70 nA | $V_{DS}$ = 0.105 V<br>$I_{DS}$ = 2.36 µA | $I_{DS}$ = 0.610 µA | $I_{DS}$ = 3.46 µA |
| 0.4 V | $V_{DS}$ = 0.185 V<br>$I_{DS}$ = 9.41 µA | $V_{DS}$ = 0.203 V<br>$I_{DS}$ = 11.9 µA | $I_{DS}$ = 12.5 µA | $I_{DS}$ = 15.6 µA |
| 0.6 V | $V_{DS}$ = 0.324 V<br>$I_{DS}$ = 24.4 µA | $V_{DS}$ = 0.332 V<br>$I_{DS}$ = 26.0 µA | $I_{DS}$ = 30.1 µA | $I_{DS}$ = 31.8 µA |
| 0.8 V | $V_{DS}$ = 0.48 V<br>$I_{DS}$ = 42.0 µA | $V_{DS}$ = 0.485 V<br>$I_{DS}$ = 42.9 µA | $I_{DS}$ = 47.9 µA | $I_{DS}$ = 48.7 µA |

(c)

In particular it is possible to evaluate the threshold voltage of the device at temperatures of 500 K and 250 K with $V_{DS}$ equal to 0.8 V and 0.05 V.

***Table 2.*** *Results extracted from trans-characteristics simulations.*

| | **Our Model** | | **FETToy Model** | | **VS-CNFET Model** | |
|---|---|---|---|---|---|---|
| $V_{DS}$ | Threshold Voltage | | Threshold Voltage | | Threshold Voltage | |
| | 250 K | 500 K | 250 K | 500 K | 250 K | 500 K |
| 0.05 V | $V_{GS}$ = 0.33 V | $V_{GS}$ = 0.26 V | $V_{GS}$ = 0.34 V | $V_{GS}$ = 0.29 V | $V_{GS}$ = 0.22 V | $V_{GS}$ = 0.15 V |
| 0.8 V | $V_{GS}$ = 0.34 V | $V_{GS}$ = 0.33 V | $V_{GS}$ = 0.38 V | $V_{GS}$ = 0.37 V | $V_{GS}$ = 0.26 V | $V_{GS}$ = 0.22 V |

Moreover, we underline how for different temperatures and different $V_{GS}$ threshold voltages for the three models are nearly coincident.

All simulations were carried out in ADS 2014 on an Asus K55VD computer which uses an Intel Core i-7 3630QM processor running at 2.4 GHz, with 4 GB of RAM memory. Moreover we have obtained almost a similarity in execution times of the simulations but our model for all simulations is faster than Stanford one. In fact the run time for our model is 0.84 s, while 1.09 s for VS-CNTFET model.

It was not possible to do this analysis for the FETToy numerical model because the tool does not provide the execution time of the simulations.

## 4. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper, we have presented a simulation study of temperature variation effects on I-V characteristics in Carbon Nanotube Field Effect Transistor. The study is carried out considering different CNTFET models proposed in the literature in order to identify the one more easily implementable in simulation software for electronic circuit design.

In particular we have compared our DC CNTFET model with the online numerical model FETToy and with the model of Stanford University, analyzing their behaviour with changing temperature.

We have compared the three considered models at 300 K with experimental data, obtaining a low agreement between for all three considered models, since, in order to have low computational cost, they do not consider both ballistic and non-ballistic transport effects.

Then, for any model, in order to study the effects of temperature on I-V characteristics, we have considered the temperature variation in the Landauer formula for the current $I_{DS}$.

We have shown how the results obtained for different temperatures (250 K and 500 K) are consistent with the three considered models, because the obtained I-V characteristics are comparable.

However, our model presented a shorter execution time, without losing accuracy.

This result allowed us to say that our model seems to be particularly suitable for CAD applications.

Currently, for any model, we are introducing the dependence on temperature of energy band gap [17] and, as only the experimental data have been measured at 300 K, we are implementing a measurement apparatus to characterize in temperature the CNTFETs behaviour, to validate the simulation results with also experimental data, measured at different temperatures.

We are also investigating about the effect of temperature [33-35] in the CNTFET-based design of analog and digital circuits.

Moreover we are studying the impact of technology on CNTFET-based circuits performance [36].

## CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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