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A Procedure to Compare CNTFET and CMOS Technologies through the Design of a SRAM Cell: A Review

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Abstract

In this paper we review in depth a procedure to compare the performance of CNTFET and MOSFET devices operating in sub-threshold region for ultra-low power applications. This aim is obtained through the design of a SRAM cell. The first design is based on our CNTFET model, while for the second one we use the BSIM4 model of the ADS library. At last the comparison between the two considered technologies are quantitatively presented, showing and discussing the improvements obtained with CNTFET technology. All simulations are carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language, avoiding so the problems presented in SPICE used in previous designs proposed in literature.

Keywords: *Nanoelectronics, Nanodevices, CNTFET, CMOS, Modelling, SRAM cell, Verilog-A.*

1. INRODUCTION

One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [1].

As it is known, the carbon nanotubes consist of a hexagonal mesh of carbon atoms wrapped in cylinder shapes. Depending on the chirality, electronic band structure of CNT changes, band gap may appear making them semiconductors, or may not appear, making them conductors.

For conventional CNTFET, also denoted as C-CNTFET, we already proposed a compact, semi-empirical model [2].

Then we introduced some improvements [3] to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A, and our model has been implemented to carry out analysis of CNTFET-based A/D circuits [4-9].

In this paper we review in depth a procedure to study the behavior of CNTFETs operating in sub-threshold region for ultra-low power applications. This aim is obtained through the design of a SRAM cell, based both on CNTFET and CMOS technology, in order to compare them.

The first design is based on our CNTFET model, while for the second one we use the BSIM4 model of the ADS library. In particular the MOSFET parameters, obtained using an evolution of previous Berkeley Predictive Technology Model (BPTM).

At last the comparison between the two considered technologies are quantitatively presented, showing the improvements obtained with CNTFET technology.

All simulations are carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [10].

The presentation of the paper is organized as follows.

In Section 2 we briefly recall our CNTFET model and the BSIM4 model for MOSFET, while Section 3 defines the experimental set-up to design a SRAM cell structure in CNTFET and CMOS technology.

The simulation results of the proposed SRAM cell design are shown in Section 3. Finally Section 4 presents a discuss of the obtained results, highlighting the comparison in terms of performance and power dissipation, while in Section 5 we report the conclusions and future developments.

2. MODELLING AND THEORY

2.1 I-V and C-V CNTFET Model

2.a I-V Model

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them. In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [11], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp} depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT}, have the expressions reported in [2-3].

2.b C-V Model

An exhaustive description of our C-V model is widely described in our Refs [7-8] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD}=q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS}=q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behaviour, it is necessary to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

In this paper we have achieved this goal using an empirical method [12], more suitable for simulations in CAD environment, obtaining the equivalent circuit of Figure 1.

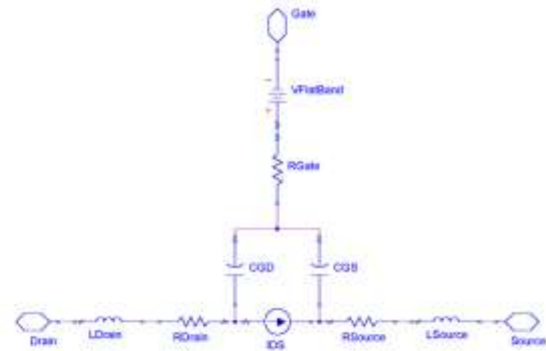

Figure 1. *Equivalent circuit of a n-type CNTFET (named as LabDis model).*

It is similar to a common MOSFET one [13] and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{Drain} and L_{Source} and the resistors R_G, R_D and R_S, in which the parasitic effect due to the electrodes are also included.

For the MOSFET model we use the **BSIM4 model** of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [14] and refers to a family of MOSFETs for integrated circuit design.

In this work BSIM4 has been used for the 32 nm technology nodes. The MOSFET parameters for BSIM4 model were obtained

by Predictive Technology Model (PTM) web site from the Nanoscale Integration and Modelling Group of Arizona State University. In particular we have selected MOSFET sizes in order to obtain output characteristics comparable to those of CNTFET.

3. EXPERIMENTAL SET-UP AND METHODOLOGY

3.1 Conventional 6T SRAM cell

A significantly large segment of modern systems on chips (SoCs) is occupied by Static Random-Access Memories (SRAMs) for their higher speed and lower power consumption.

A 6T SRAM cell structure is shown in Figure 2. It is the same for both CNTFET and MOSFET technology.

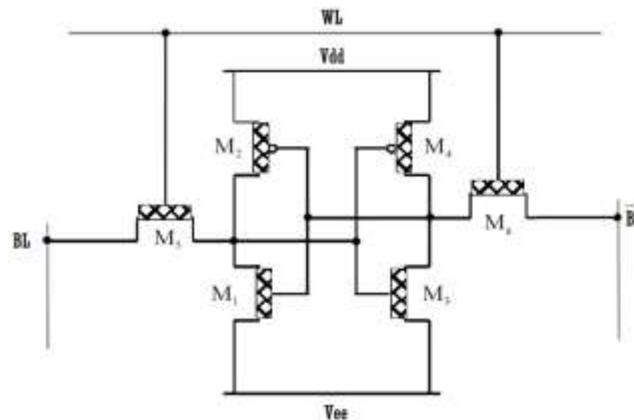

***Figure 2**. A 6T SRAM cell structure.*

In Figure 2 there are four transistors (M1, M2, M3, M4) that form a pair of inverters. This storage cell is used to store a bit of information, in particular it has two stable states which are used to denote "0" and "1". The other two transistors (M5 and M6) are called the access transistors because contribute to control the access to the cross coupled unit formed by the inverters during read and write operations. So typically, it takes six transistors to store one memory bit. These access transistors are controlled by the word line (WL) which allows the two bit lines BL and $\overline{BL}$ to access the memory elements [15-16].

The two bit lines BL and $\overline{BL}$ are used to transfer data for both read and write operations and their presence improves noise margins over a single bit line. The symmetric circuit structure allows for accessing a memory location much faster than in a DRAM.

3.2 6T SRAM Cell Operation

3.2.1 Write Operation

The start of a write cycle begins by applying the value to be written and its complement to the bit lines. In order to write a '0', we would apply a '0' to the bit line BL and its complement '1' to the $\overline{BL}$. Vice versa to write a '1'. Then WL is made high and the value that is to be stored is latched in.

3.2.2 Read Operation

The read cycle is started by asserting the word line WL, enabling both the access transistors M5 and M6. The second step occurs when the values stored in D and $\overline{D}$ are transferred to the bit lines BL and $\overline{BL}$ through M1 and M6. On the BL side, the transistors M4 and M5 pull the bit line towards VDD (when a "1" is stored at D). If the content of the memory was a 0, the reverse would happen and $\overline{BL}$ would be pulled towards 1 and BL towards 0.

3.2.3 Idle State

For the idle state, the word line is not asserted and the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters will continue to reinforce each other as long as they are disconnected from any external circuits.

3.3 Schematic of CNTFET-Based 6T SRAM Cell in ADS

First of all, we want to underline that in the following simulations, for all CNTFETs we have assumed a channel length equal to 32 nm and a transistor width W equal to 64 nm for M1, M3, M5 and M6 and equal to 80 nm for M2 and M4, in order to have comparable results with References [17-18]. All CNFETs use nanotubes as channel, having chirality (19, 0). In fact, the diameter of CNT, dependent on chirality, is 1.49 nm and therefore the threshold voltage of the CNFETs using (19, 0) CNTs is 0.289 V. These values in [17] have been identified as optimal values during read operation of the stored data or during write operation of new data in the memory cell.

The schematic of CNTFET based SRAM cell is represented in Figure 3. Moreover a dual power is used to make the cell output waveforms symmetric.

In this schematic, seven ports are inserted to associate the input and output signals of the cell to the appropriate input and output pins of the symbol, shown in Figure 4 related to the schematic. In fact, this symbol allows to compact the entire circuit into a single block. In this way, this block can be invoked by the ADS library and used in more complex circuits, simplifying the topology.

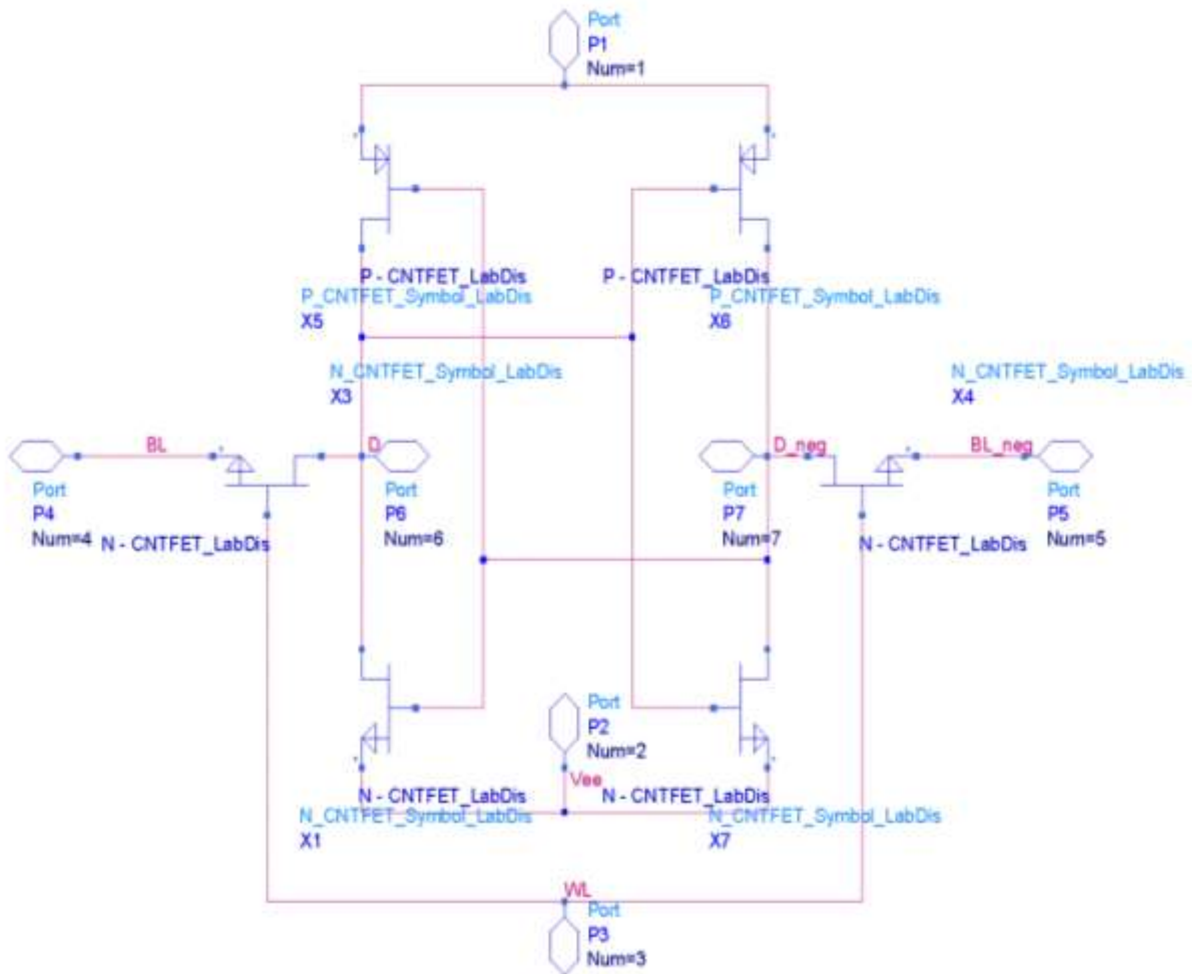

Figure 3. *Schematic of CNTFET based SRAM Cell in ADS.*

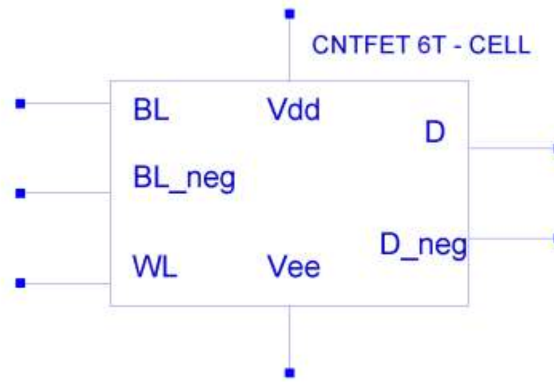

Figure 4. CNTFET 6T SRAM symbol.

3.4 Schematic of CMOS-Based 6T SRAM Cell in ADS

The schematic of CMOS based SRAM cell, is shown in Figure 5, where the MOSFET12 and the MOSFET13 are PMOS, while the remaining are all NMOS. The conversion from NMOS to PMOS is done by setting the "NMOS" parameter to "NO" and "PMOS" parameter to "YES". Also in this case dual power is used to make the cell output waveforms symmetric. In Figure 6 the CMOS 6T SRAM symbol related to the schematic is represented.

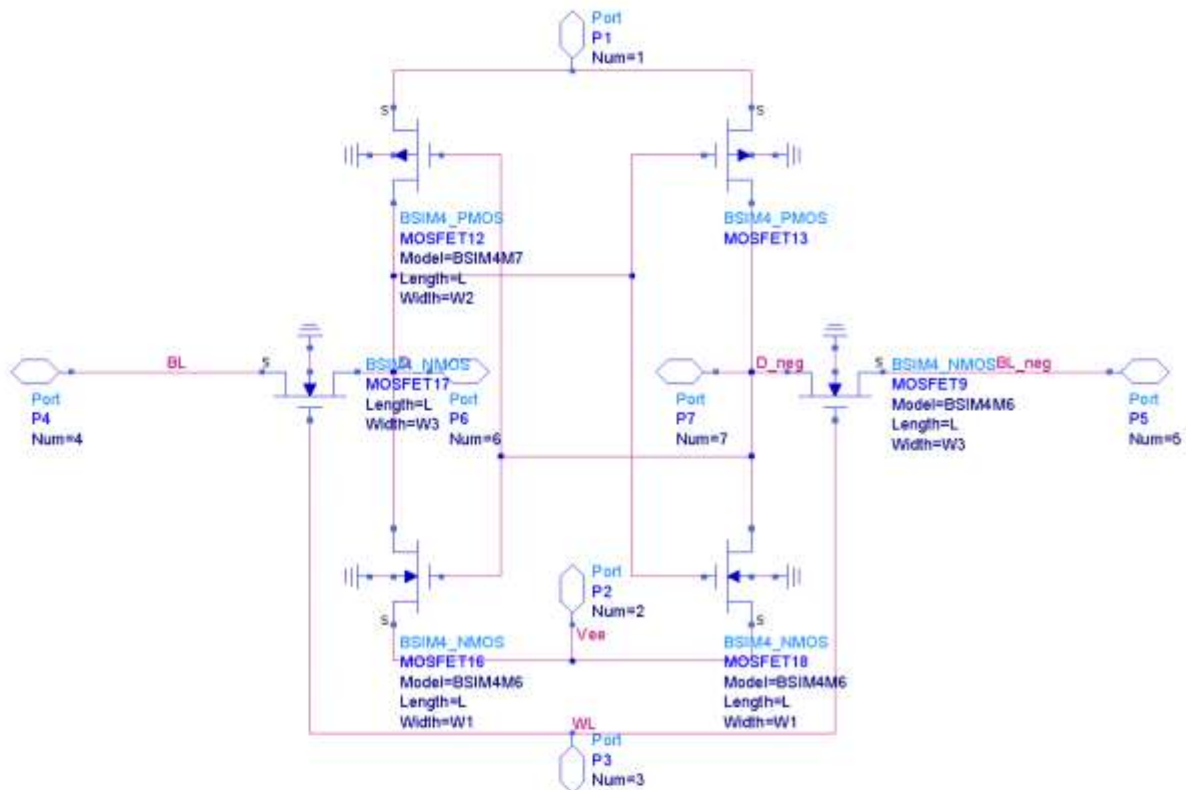

Figure 5. Schematic of CMOS-based SRAM Cell in ADS.

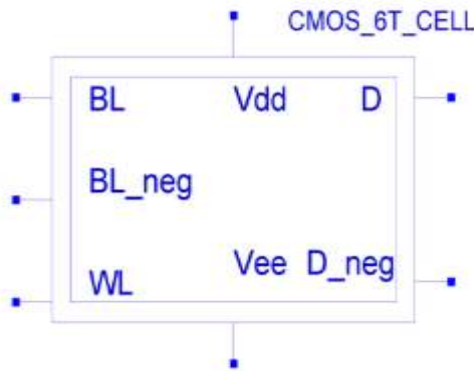

Figure 6. *CMOS 6T SRAM symbol.*

3.5 CNTFET-Based 6T SRAM Cell: Transcaracteristic and Gain Simulations

The simulated circuit in ADS for the calculation of the transcharacteristics and the gain of the CNTFET based SRAM 6T cell is shown in Figure 7.

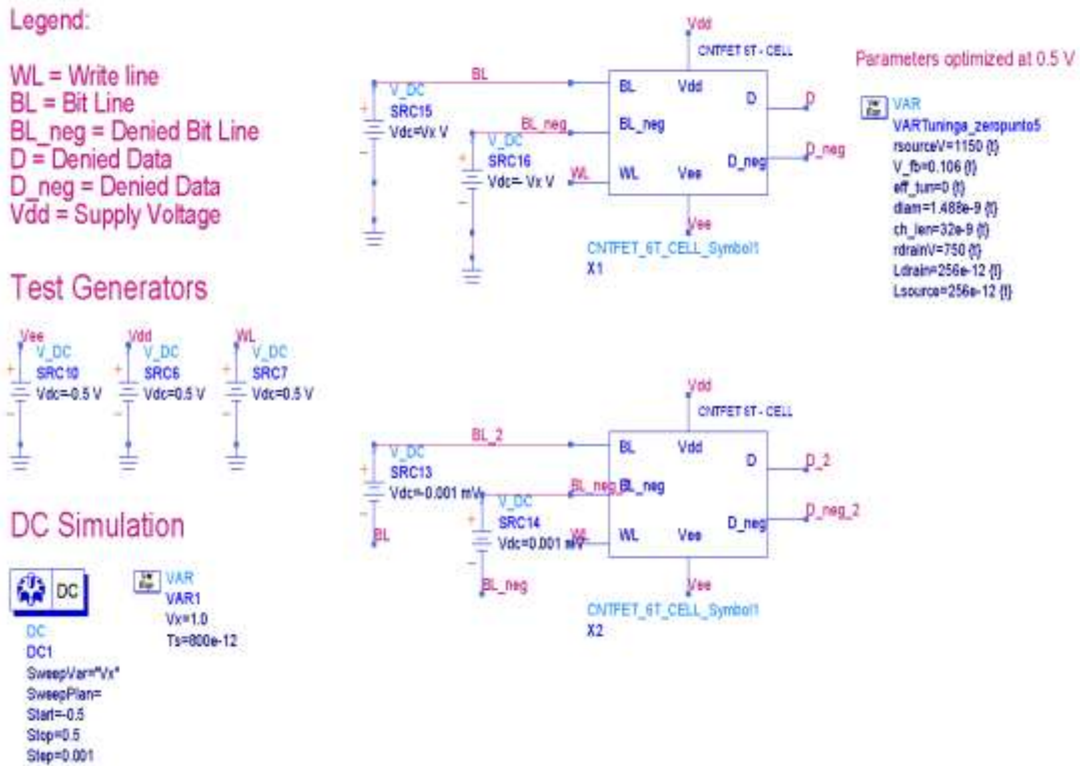

Figure 7. *CNTFET based SRAM 6T cell: circuit for transcharacteristic and gain calculation.*

Figure 8 shows the transcharacteristics obtained for a supply voltage of ± 0.5 V, while Figure 9 the differential gain curves in semi-logarithmic scale obtained for a supply voltage of ± 0.5 V.

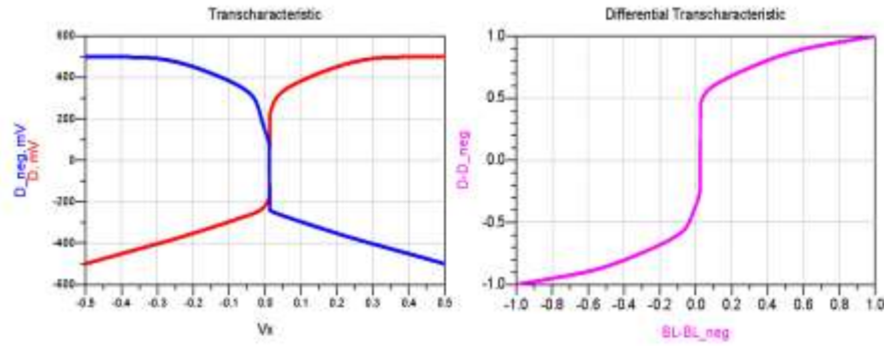

Figure 8. *Transcharacteristics for a supply voltage of ± 0.5 V.*

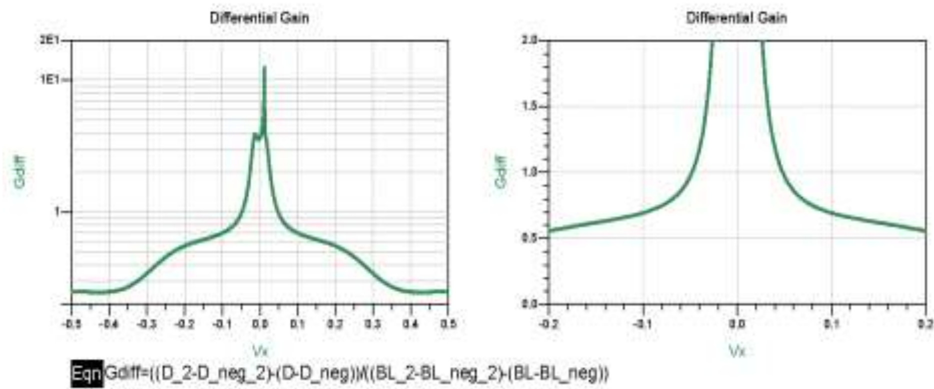

Figure 9. *Differential gain for a supply voltage of ± 0.5 V.*

The graph shown in Figure 10 allows the calculation of the logical thresholds whose positions are identified by two markers.

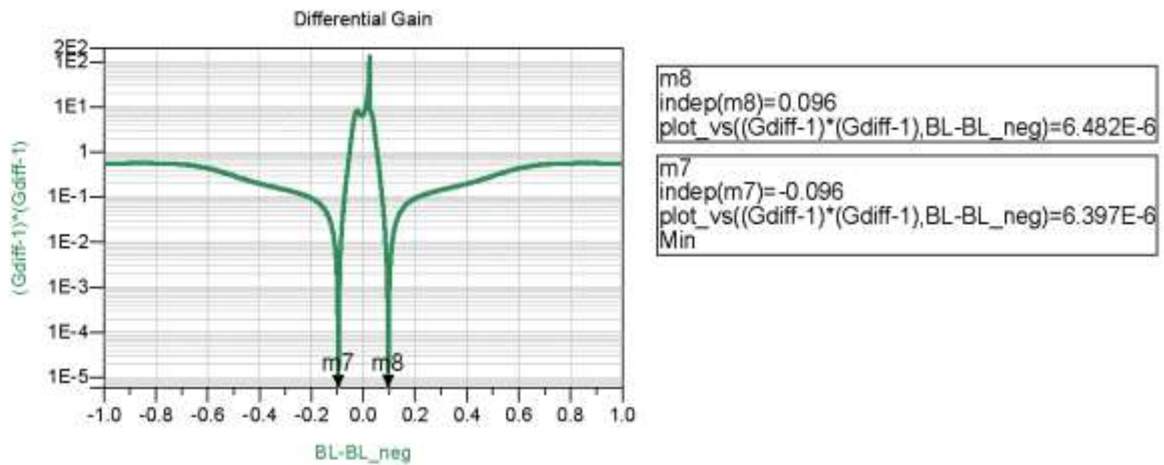

Figure 10. *Calculation of logical thresholds CNTFET based SRAM 6T cell (supply voltage of ± 0.5 V).*

Figure 11 shows the characteristics of the transcription. The markers are positioned to identify the logical thresholds and consequently the logical swing.

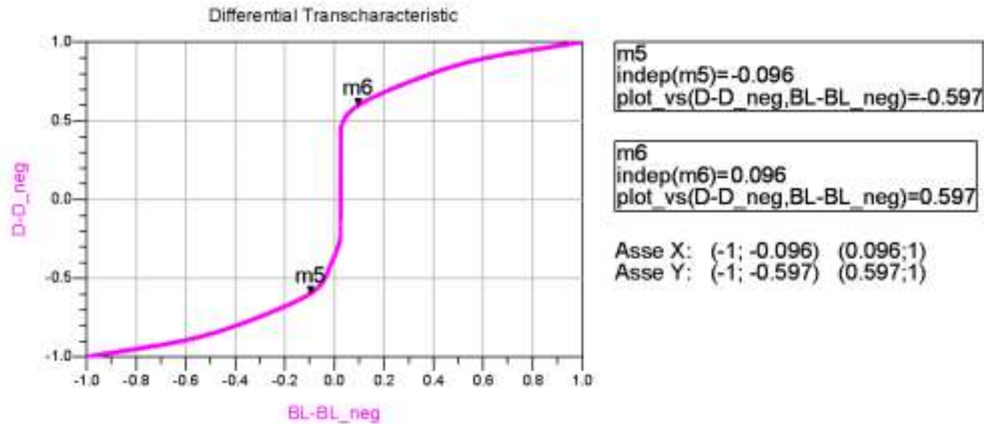

Figure 11. *CNTFET based SRAM 6T: identification of the logical swing (supply voltage of ± 0.5 V).*

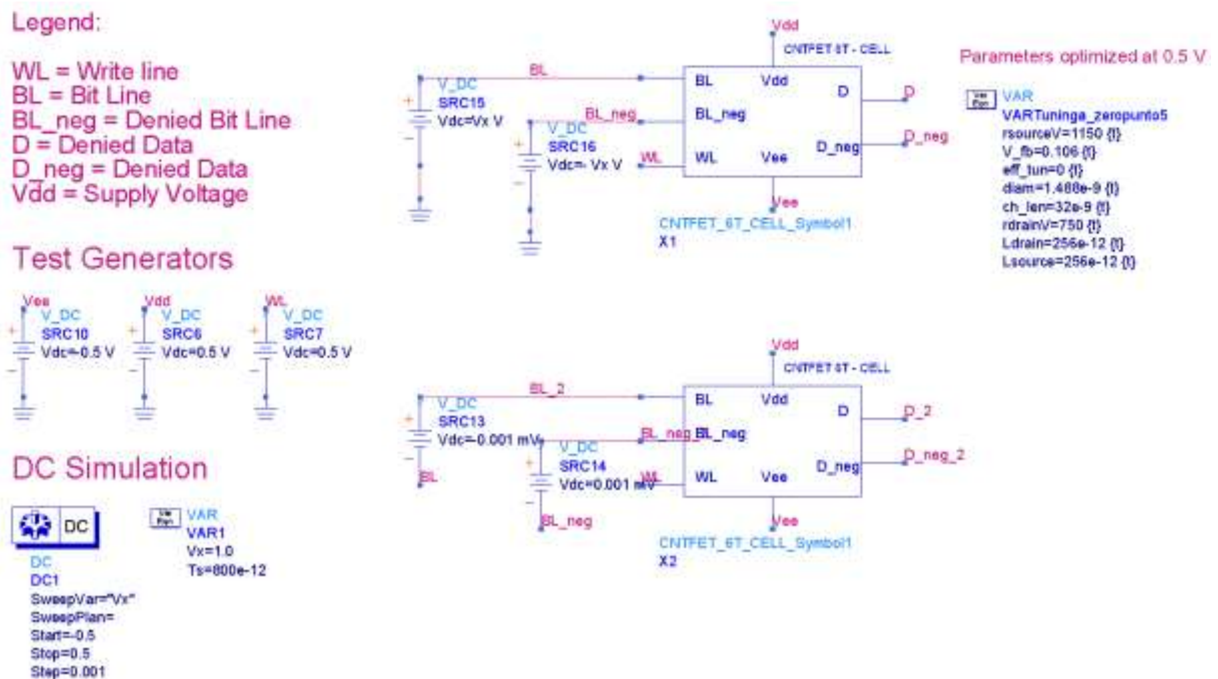

Figure 12. *CNTFET based SRAM 6T cells in cascade for transient simulations.*

3.6 CNTFET-based 6T SRAM cell: Ttransient Simulations

Figure 12 shows the circuit realized to carry out the transient simulations.

We have not used a single cell: in fact to make the simulation approximable to a realistic behaviour, a cascade of 6T cells must be realized. Each cell serves as a load for the previous one. The output signals of each cell represent the input signals of the next cell. This ensures that the trapezoidal wave signal, supplied at the input of the first cell, is not exactly identical to the one arriving at the third cell input. In fact, the trapezoidal signal has been shaped appropriately making it comparable to a possible real signal.

In the circuit of Figure 12 the supply voltage is equal to ± 0.5 V and the working frequency is 2.2 GHz. However we have simulated this circuit in ADS considering the following four cases:

- supply voltage = ± 0.5 V; working frequency = 2.2 GHz

- supply voltage = ± 0.5 V; working frequency = 3.84 GHz
- supply voltage = ± 0.3 V; working frequency = 2.2 GHz
- supply voltage = ± 0.3 V; working frequency = 3.84 GHz

Figure 13 shows the output waveform of the first cell of the cascade.

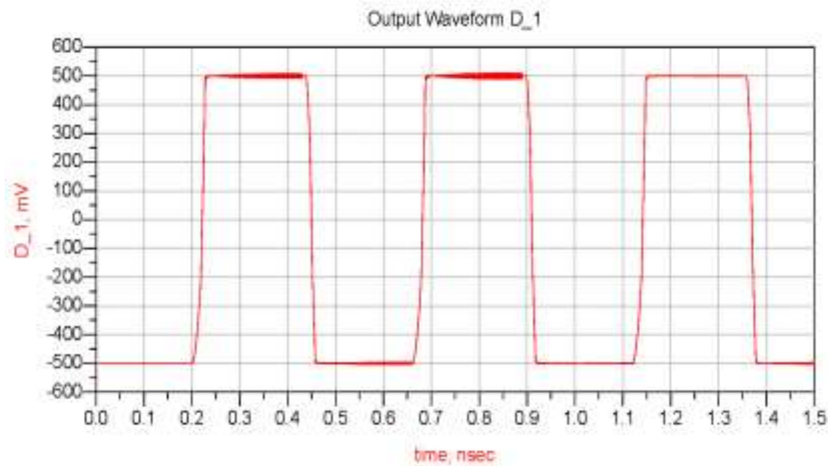

Figure 13. *Output waveform of the first cell of the cascade (supply voltage = ± 0.5 V; working frequency = 2.2 GHz).*

It is possible easily to determine the output waveform of any cell of the cascade and, in order not to make the discussion heavier, we will limit ourselves to reporting the waveform at the exit of the third cell under test. In particular Figure 14 shows the output waveform of the third cell of the cascade for a supply voltage = ± 0.5 V and working frequency = 3.84 GHz.

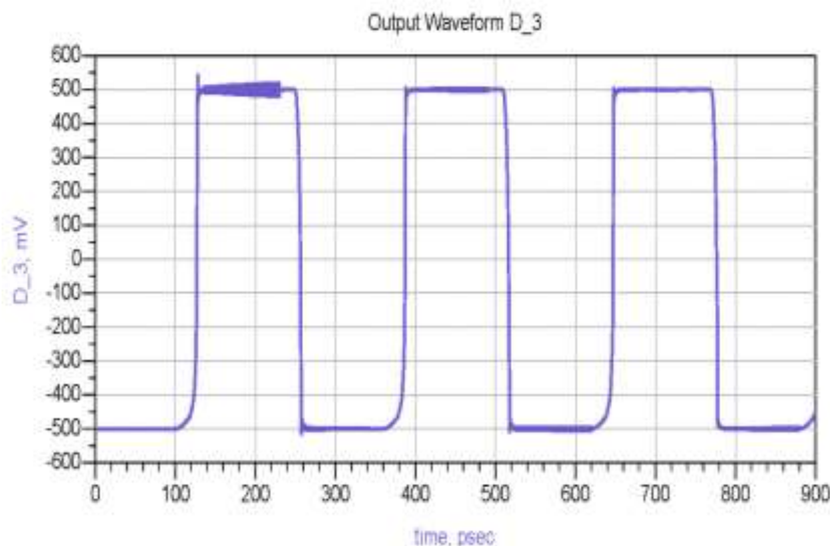

Figure 14. *Output waveform of the third cell of the cascade (supply voltage = ± 0.5 V; working frequency = 3.84 GHz).*

In this way it is possible to evaluate the rising edges of the signals passing through the cascaded cells, reported in Figure 15, for a working frequency equal to 3.84 GHz, and a supply voltage of ± 0.5 V.

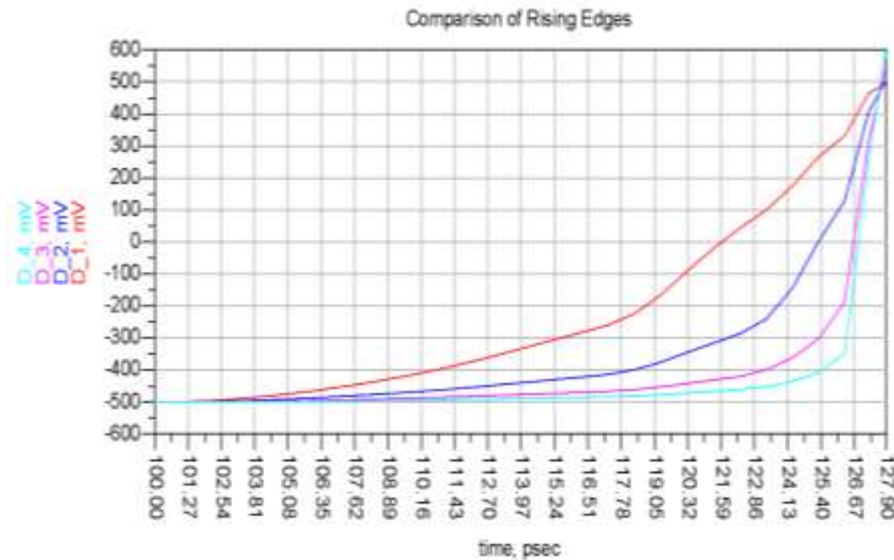

__Figure 15.__ Rising edges of the signals passing through the cascade (supply voltage = ± 0.5 V; working frequency = 3.84 GHz).

3.7 CNTFET-based 6T SRAM Cell: Power Analysis

Figure 16 shows the trend of the current relative to the power supply. In order to not weight the treatment, we have only reported the graphs related to the following case, i.e. supply voltage = ± 0.5 V and working frequency = 3.84 GHz.

In this way it is possible to determine the values of the integrated current in a period, the values of the energy and the power.

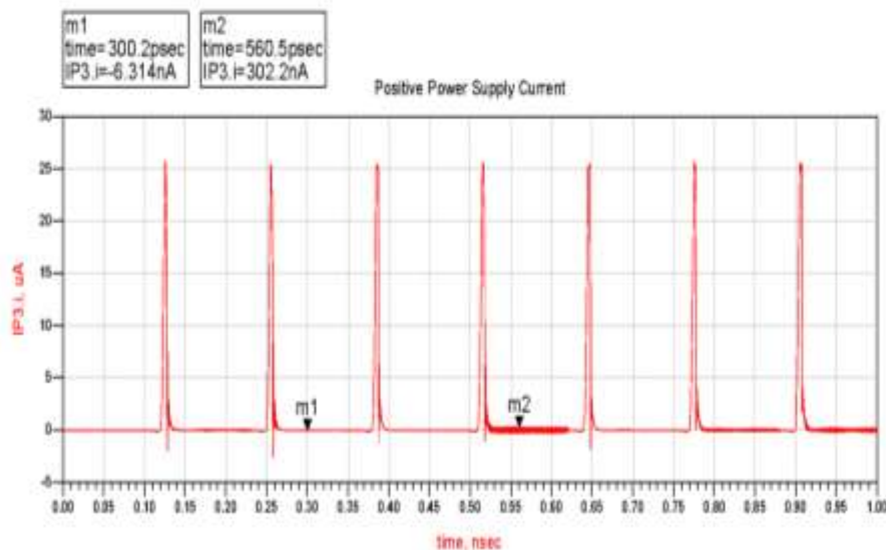

__Figure 16.__ Trend of the current relative to the power supply (± 0.5 V and 3.84 GHz).

3.8 CMOS-Based 6T SRAM Cell

To compare the performance of the implemented SRAM in CNTFET technology with the same in CMOS technology, we have proceeded in the same way already described. In particular in Figure 17 there are two circuits that have been implemented in ADS to study the operation of CMOS based 6T SRAM cell for transcaracteristic and gain simulations.

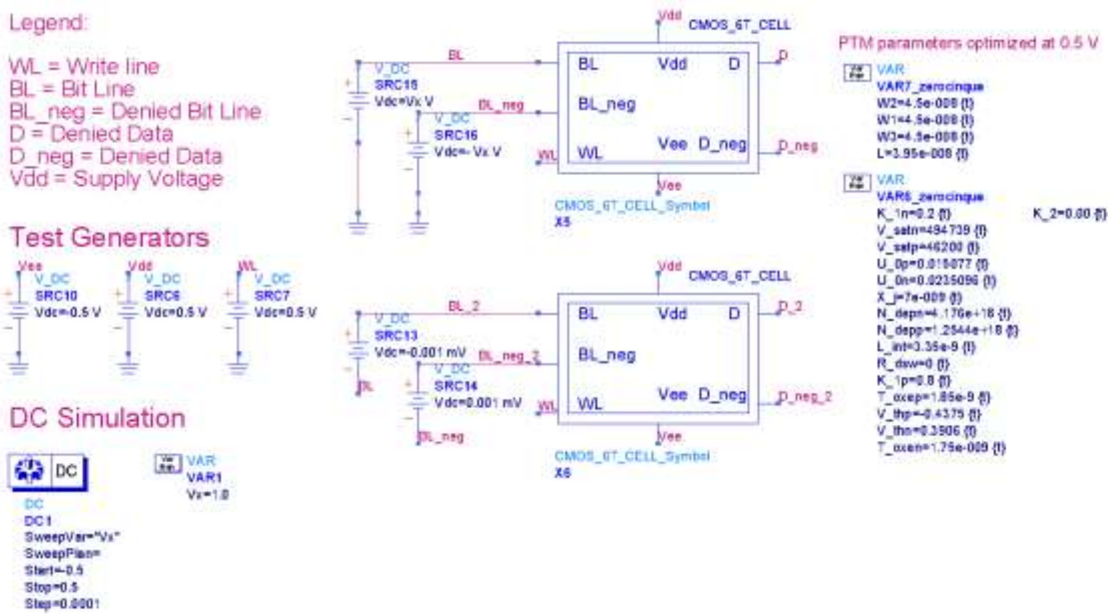

Figure 17. CMOS-based SRAM 6T cell: circuit for transcharacteristic and gain calculation.

The first circuit is interested by the two signals BL and BL_neg, which must necessarily be in phase opposition to allow the cell to work correctly. The other circuit is identical to this one, but in this case a small differential input signal is applied.

Figure 18 shows the circuit realized to carry out the transient simulations. In this circuit we have considered a supply voltage equal to ± 0.5 V and a working frequency of 2.2 GHz. Of course it is possible considered the other cases, examined previously.

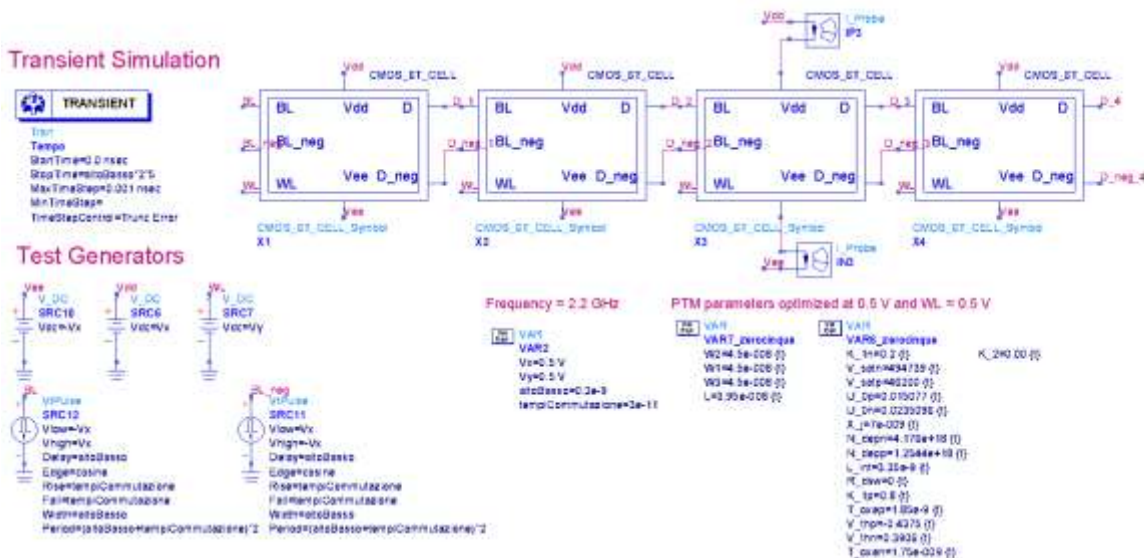

Figure 18. CMOS based SRAM 6T cells in cascade for transient simulation.

In order to not weight the treatment, we have only reported the graphs related to the rising edges of the signals passing through the cascaded cells, reported in Figure 19, for a supply voltage of ± 0.5 V and for a working frequency equal to 3.84 GHz, while in Figure 20 we have reported the trend of the current relative to the power

supply in the same work condition.

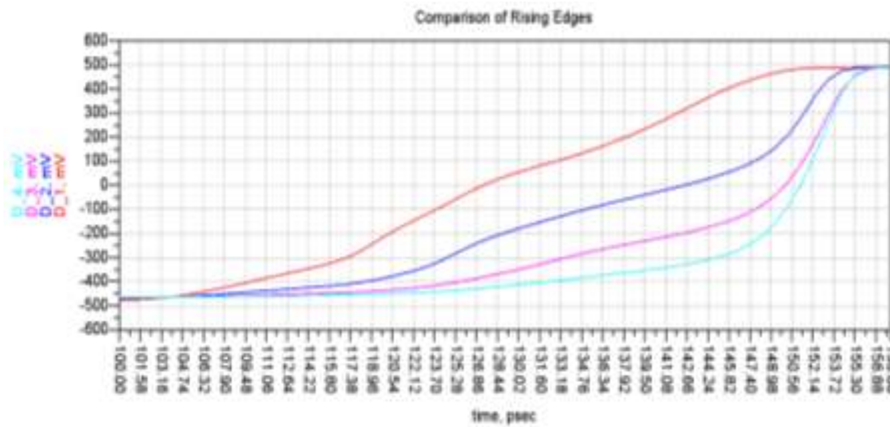

__Figure 19.__ Rising edges of the signals passing through the cascade (supply voltage = ± 0.5 V; working frequency = 3.84 GHz).

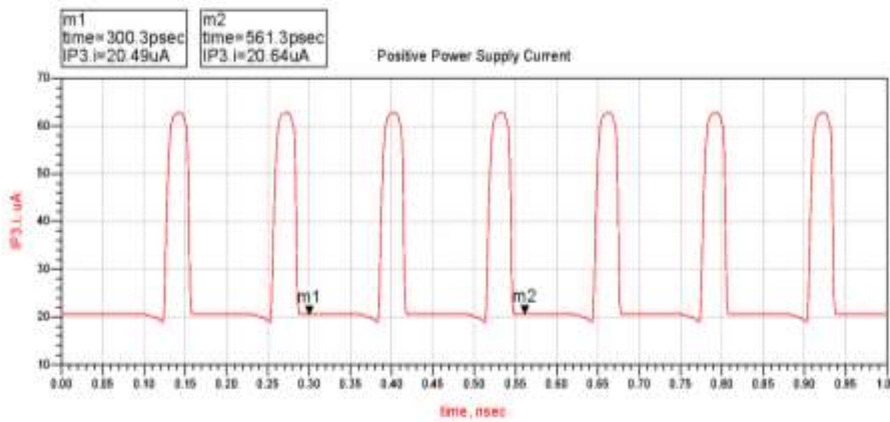

__Figure 20.__ Trend of the current relative to the power supply (± 0.5 V and 3.84 GHz).

In this way it is possible to determine the values of the integrated current in a period, the values of the energy and the power, as described for CNTFET design.

4. RESULTS AND DISCUSSION

The obtained results can be summarized through the following Tables, which allow us to do a comparative analysis between CNTFET and CMOS technologies.
In particular the values obtained from the simulations are shown in Table 1, 2, 3 and 4, in which we reported the power and the rising time for both technologies, considering also the simulation results for:

1. supply voltage = ± 0.5 V; working frequency = 3.84 GHz
2. supply voltage = ± 0.3 V; working frequency = 2.2 GHz
3. supply voltage = ± 0.5 V; working frequency = 2.2 GHz.

__Table 1__. Power and rising time values for the designed SRAM 6T cell (Supply Voltage= ± 0.5 V and frequency = 2.2 GHz).

Technology	Power (μW)	Rising Time (ps)
CMOS 45 nm	12.68	28.8
CNTFET 32 nm	0.27	4.2

Table 2. *Power and rising time values for the designed SRAM 6T cell (Supply Voltage= ± 0.3 V and frequency = 2.2 GHz).*

Technology	Power (μW)	Rising Time (ps)
CMOS 45 nm	1.44	35
CNTFET 32 nm	0.04	18.1

Table 3. *Power and rising time values for the designed SRAM 6T cell (Supply Voltage= ± 0.5 V and frequency = 3.84 GHz).*

Technology	Power (μW)	Rising Time (ps)
CMOS 45 nm	14.4	28.8
CNTFET 32 nm	0.47	4.2

Table 4. *Power and rising time values for the designed SRAM 6T cell (Supply Voltage= ± 0.3 V and frequency = 3.84 GHz).*

Technology	Power (μW)	Rising Time (ps)
CMOS 45 nm	2	35
CNTFET 32 nm	0.082	18.2

As far as the power dissipation is concerned, it is possible to observe that both technologies allow to realize low power devices.

Another evidence has been given by the fact that the maximum benefits are achieved for different quiescent points between one technology and the other. In particular we have noticed that the quiescent point of CNTFET needs of a bias voltage slightly high for the correct operability due to the presence of a flat band voltage higher that increases the threshold voltage. Therefore power requirements slightly greater are needed.

5. CONCLUSIONS AND FUTURE DEVELOPMENTS

We reviewed in depth a procedure to compare the performance of CNTFET and MOSFET devices operating in sub-threshold region for ultra-low power applications, through the design of a 6T SRAM cell.

We observed that the memory cell realized with CNTFET allows to reach very high working frequencies, always guaranteeing a reliable and little distorted signal. The static analysis of the cell has allowed the determination of the logical thresholds, which in CNTFET technology are more restricted than those obtained in CMOS technology.

The simulations of the SRAM cell in CMOS technology have shown a good operation up to near 4 GHz frequencies, beyond which the signal undergoes strong alterations, becoming a first triangular approximation signal.

We intend to repeat the proposed simulations using other CNTFET models such the Stanford model [19-22] in order to compare results.

Currently we are working to study the effect of temperature [23-25] and of noise in other circuits based on CNTFETs [26].

Moreover we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [27-28] and the impact of technology on CNTFET and CMOS-based circuits performance [29-30].

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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