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Low-Power High-Frequency Phase Frequency Detector Based on Carbon Nano-Tube FET with Zero Dead-Zone for CPPLL

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Abstract

Achieving low power consumption and low delay are the most important goals that efforts have been made to reach. In this paper, the process of designing and optimizing the Phase Frequency Detector (PFD) performance at the integrated circuits (IC) level has been proposed using carbon nanotubes. In the proposed method, by using carbon nanotube transistors, improvements have been made in the output parameters of the phase detector. Failure to use flip-flops and the simple circuit structure will significantly increase speed and reduce power consumption. Post-layout simulation for 180nm CMOS technology and simulation results for 32nm Carbon Nanotube Field-Effect Transistor (CNTFET) technology is presented. The proposed CMOS 28T phase detector circuit, by injecting 30mV peak-to-peak power supply noise has 5× better operating frequency of the conventional circuit, and it has a 10% improvement in power consumption of the conventional one. Also, with carbon nanotubes, the frequency has increased 4 times, and the power consumption has improved significantly. In this case, the power consumption is 1.76 microwatts, and the operating frequency is 20 GHz. Open-loop design and elimination of the reset path, and attention to delays to remove the dead zone are the proposed circuit's top features compared with the traditional design methods.

Keywords: *Phase-frequency detector, Zero dead-zone, Low power consumption, High frequency, Carbon nanotubes.*

1. INRODUCTION

PLLs are widely used in micro-processors, digital signal processors, and communication systems. The purpose of new research related to the PLLs is the fast access to the locking process, lower jitter, lower power, and higher operational frequency [1]. PLL is a feedback system that receives the reference signal and, using the feedback path, performs the control process for the output signal to be synchronous in terms of phase and frequency with the reference signal [1]. In this mode, the PLL is in the locked position. The output signal of the oscillator is constantly monitored, and an error signal will be generated in case of a phase and frequency deviation between this signal and the reference signal for the oscillator to become synchronous with the reference signal. This error signal is generated by the phase-frequency detector and transferred to the oscillator (which can be controlled by voltage or current) so that the oscillator can adjust the output signal using that signal. Figure 1 indicates the role of the frequency synthesizer in a typical transmitter-receiver structure, which is the ultra-wideband (UWB), and Figure 2 is the Structure of frequency synthesizer-based PLL.

A circuit that can detect the deviation of both phase and frequency can be very helpful since it can increase the PLL's locking range and locking speed. The phase-frequency detector is a block that detects the deviation of the phase and frequency of its inputs and generates a sequence of UP and DOWN pulses with some limitations [2].

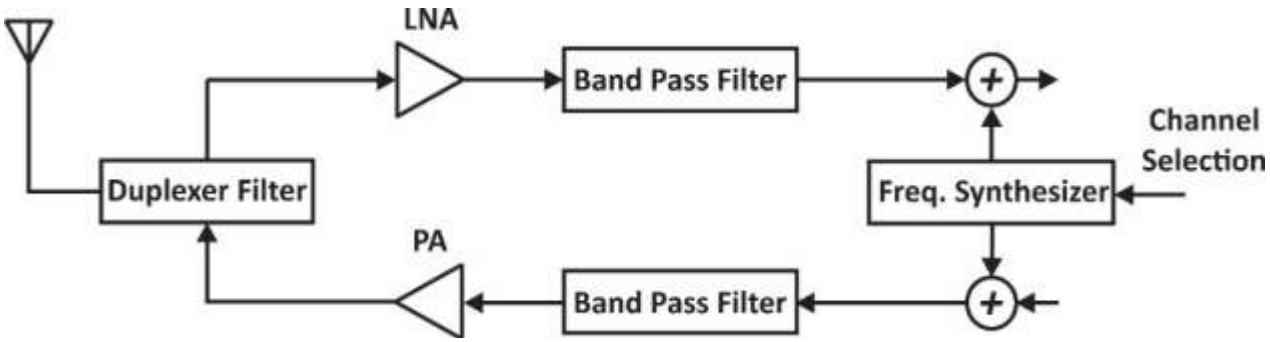

Figure 1. *Structure of a typical transmitter-receiver [1].*

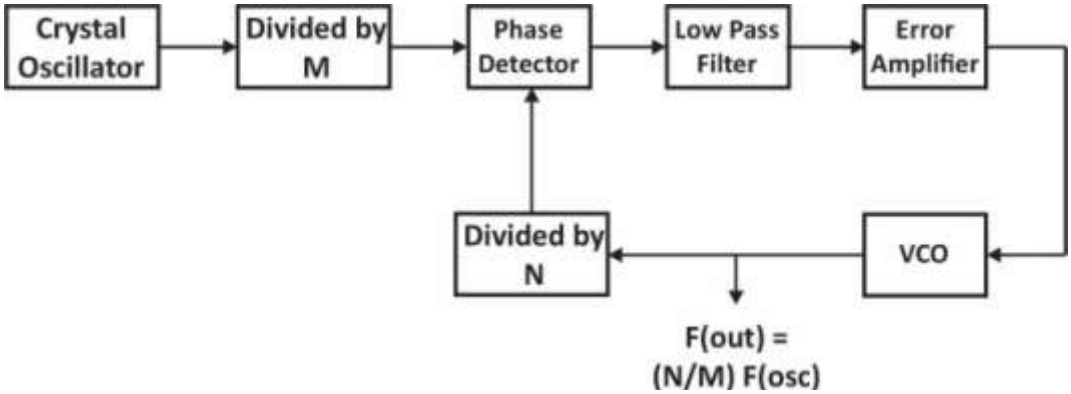

Figure 2. *Structure of frequency synthesizer based PLL [1].*

Figure 3 is the conventional Structure of the phase frequency detector with operation and output results. PFDs are generally designed in two forms, open-loop and closed-loop. In closed-loop circuits, the speed is severely limited since sequential elements are used to detect the edge of the signals. Also, adding a divider increases the jitter or phase noise in the time and frequency domains, respectively. One of the problems of the closed-loop circuit is that some of the rising edges will be missed during the detection. This problem occurs when the increasing edge overlaps the reset signal [3-7]. In [8], the achieved maximum frequency of operation is 3.44 GHz which is suitable for high reference clocked fast settling PLLs and has an open loop structure. The proposed Structure of [9] uses two D flip-flops in true single-phase clock (TSPC) logic and an AND gate in gate-diffusion input (GDI) logic. Using just 16 transistors achieves 110 μW power consumption. In [10], a precharged phase frequency detector (PPFD) with improved output characteristics for phase locked loop (PLL) has been proposed with a power consumption of 285 μW in 180nm CMOS technology. In [11, 12] phase detector is utilized, and a variable-delay element is used in the loop of ECDLL and PLL, respectively. In [13, 14], an open-loop PD is presented that obtains high speed, wide locking range, and low perturbation by omitting the sequential circuits. Although, the power consumption of this circuit is high due to the rotational current in the main transistors of PD when both of the input signals are one.

In the conventional phase frequency detectors, a reset path exists, and there are delays in this path that have a direct relation to the dead zone and the operating frequency according to the relation [1, 15]:

$$F_{PFD(max)} = \frac{1}{2\times\tau 1} \quad (1)$$

$$Dead\text{-}Zone = \frac{\pm\tau\pi}{T} \quad (2)$$

where τ1 is the additional delay added to the PFD, τ is the rise time, and T is the reference period [15].

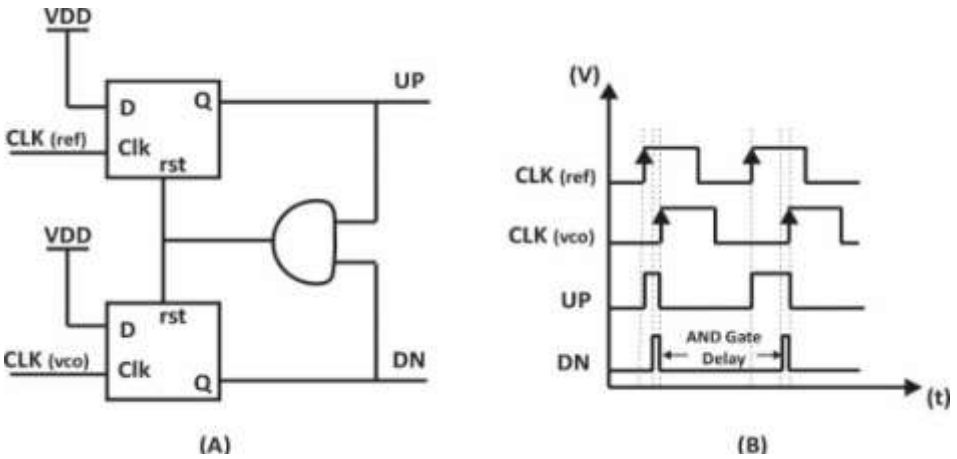

Figure 3. *Conventional PFD Operation, (a) Schematic (b) Operation and results.*

The smaller the dead zone, the lower the loop output jitter. The proposed phase detector in this paper has a high speed due to the employment of an open-loop structure and a straightforward structure; the power consumption and noise level in the proposed circuit are sharply reduced using carbon nanotube field effect transistors.

2. A BRIEF REVIEW OF CNTFETs

Carbon nanotubes are carbon allotropes with cylindrically rolled-up graphite-like structural characteristics. They also display the attributes of semiconductors and metals. The property under consideration will affect the classification in Table 1. For instance, "they can be classified into Armchair, Zigzag, and Chiral types" [16-22] based on their structural makeup. Additionally, layering is used to categorize structural types; thus, a structure may be mono-walled or multi-walled. They can exhibit the characteristics of a metal or a semiconductor due to their capacity to reach the configuration mentioned above. As shown in Figure 4 and quantified by the chirality vector (C), which is defined by equation 1, these connections between sheets are a measure

$$C = nX_1 + mX_2 \quad (3)$$

The final structure depends on the "relationship between (n, m); for instance, if n = m, the structure is an armchair; if n=m and m = 0, it is a zigzag; and if n > m or n m, it is chiral" [21]. In equation n (1), the unit vectors are X_1 and X_2. The "suggested circuit is created using the zigzag structure, with n = 19 and m = 0. (19, 0)" [22, 23].

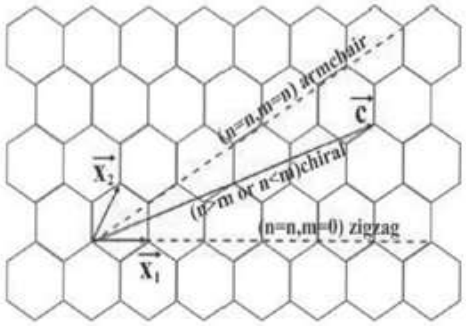

Figure 4. *Representation of Chiral Vector.*

In the literature, three different CNTFET device types have been mentioned. Schottky barrier CNTFETs, MOSFET-like CNTFETs, and band-to-band tunneling CNTFETs are the names of these devices (T-CNTFET). It has been used in the implementation of logic circuits due to M-operational CNTFET's and intrinsic similarities to MOSFET [24-27]. As it mentioned, in the new designs of the phase detector, the reset path has been removed, and the proposed circuit is an open loop so that the power consumption is lower and the lower dead zone can be reached.

Table 1. *CNTFET Parameters, values and their description.*

CNTFET Description	CNTFET Parameter	Value
Gate supply voltage	Supply	0.9
Physical channel length	Lch	3.20E-08
The S/D tube's doped Fermi level	Efi	0.6
In the intrinsic CNT channel, the mean free path	Lgeff	1.00E-07
The size of the source-side extension of doped CNT	Lss	3.20E-08
Gate oxide dielectric constant	Kox	16
How far the doped CNT drain-side extension extends	Ldd	3.20E-08
Number of CNTs	Tubes	3
Temperature	Temp	25
The capacitance between the channel and substrate	Csub	4.00E-11
The high-k top gate dielectric material's thickness	Tox	4.00E-09
The distance between the centers of two adjacent CNTs	Pitch	2.00E-09

DFF-based phase detectors can have a lower operating frequency due to the DFF function. Therefore, this block has been removed in new designers, or TSPC logic has been used to reach a higher working frequency. Next, the results show that removing the reset path and controlling the delays from input to output can achieve a shallow dead zone (close to zero) and a high operating frequency in cases of similar technology. Also, using carbon nanotube transistors' capability, it reached much higher operating frequencies.

3. PROPOSED PHASE DETECTOR

In the proposed circuit, two separate paths are used for the signals UP and DN, shown in Figure [4]. Here, the intermediate signal is used to generate the final signal, which is shown in Figure 4. a. for the up signal and in Figure 4. b. for the DN signal. The waveforms related to this circuit in Figure 4 indicate the UP and DN signals direction. Consider a situation where A is ahead of B. When both the A and B are "0" the intermediate signal output will be "1" With A changing from "0" to "1" the intermediate signal will be "0" When both signals are "1" the signal output will stay in the previous situation. And finally, when A is "0" and B is "1", the production of the signal will be "0". The generation of this intermediate signal readily performs the detection between two signals. To better understand this matter, Table 2 and Table 3 shows the output signal of UP and DN with changes.

The same relationships hold when B is ahead of A, this can be seen in Figure 5.

After generating the intermediate signal, to develop the output signals, it is only necessary to AND the intermediate signals with the A and B inputs to obtain the desired output. This circuit is shown in Figure 3 for UP and DN signals.

Table 2. *The output signal of UP circuit.*

A	A	B	Intermediate (UP)
0	0	0	1
1	1	0	0
1	1	1	Previous State
0	0	1	0

Table 3. *The output signal of DN circuit.*

A	B	Intermediate (DN)
0	0	1
1	0	Previous State
1	1	0
0	1	0

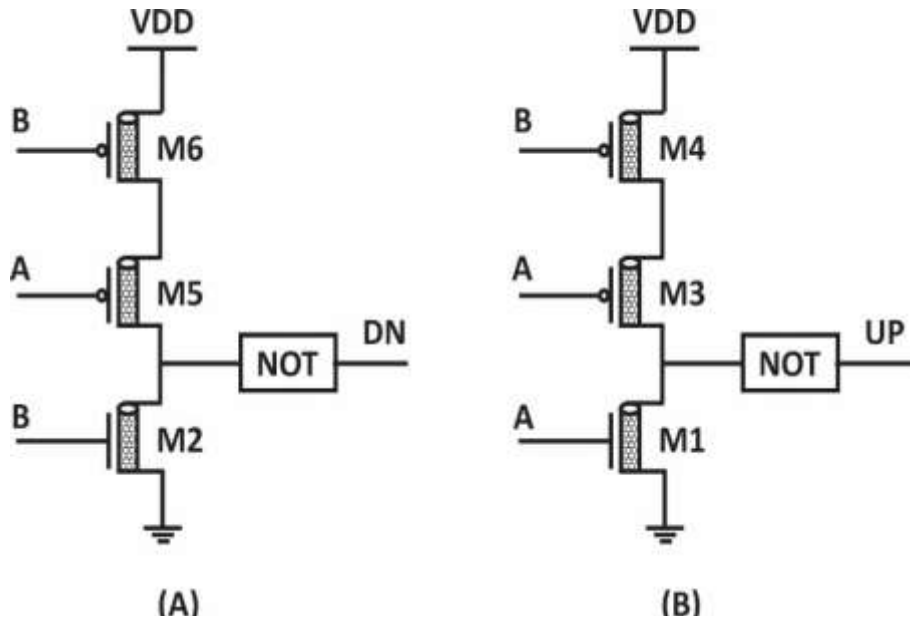

Figure 4. *(a) UP intermediate signal (b) DN intermediate signal.*

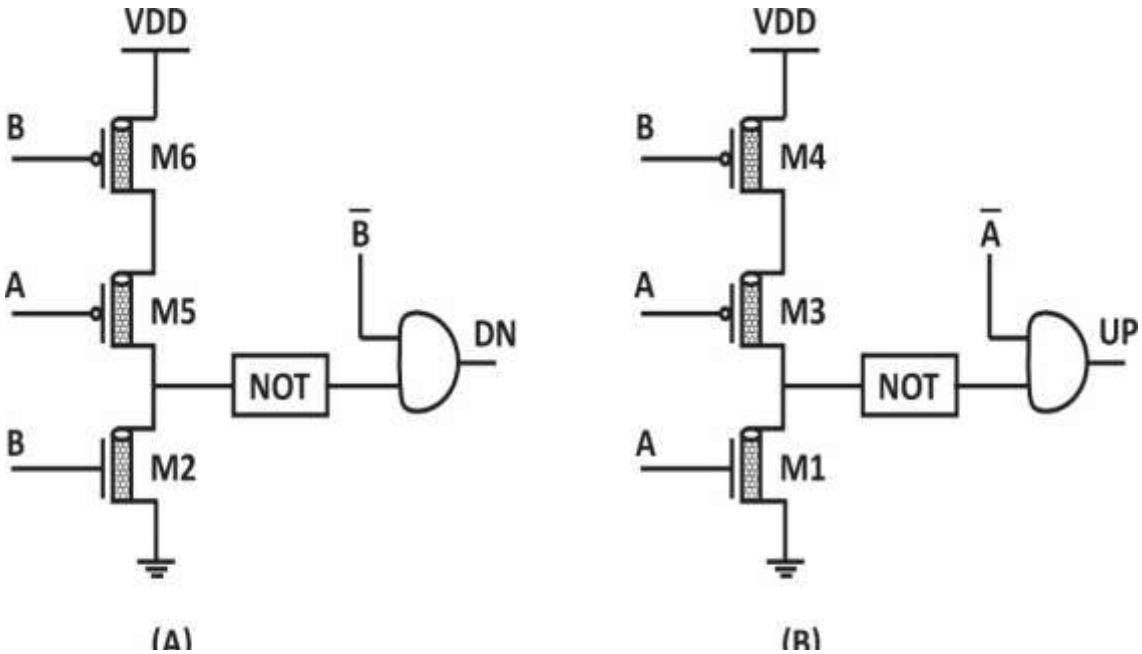

Figure 5. *(a) UP signal and (b) DN signal.*

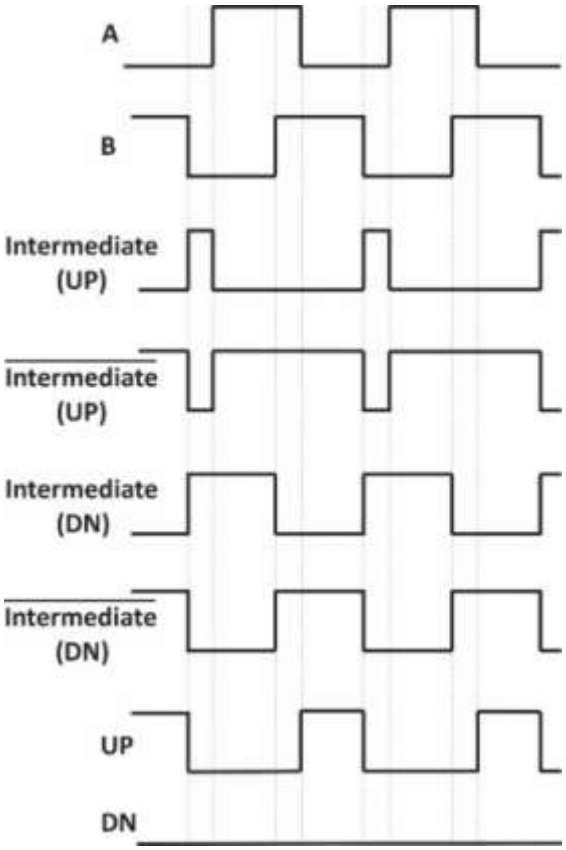

Figure 6. *UP and DN signal generation.*

Figures 6 and 7 are UP and DN signal generation when B and A are pre-phase, respectively. Employing this idea improves speed and accuracy. Although, the above circuit has a fundamental problem. When the deviation between the inputs is low, the output signal can't follow these changes. In other words, if the input phase difference is less than a detectable value, then PD output can't be a function of. The change range between $+\Delta\emptyset$ to $-\Delta\emptyset$ is called the dead zone. The worst effect of the dead zone on the performance of a PD is the time of loop lock time. A delay has to be inserted in the intermediate signal path so that the perturbation of the loop can be omitted in the locking range. The output signal will be applied to the charge pump part from the phase detector circuit, which will effectively charge and discharge the capacitor. This problem can be solved by using a delay.

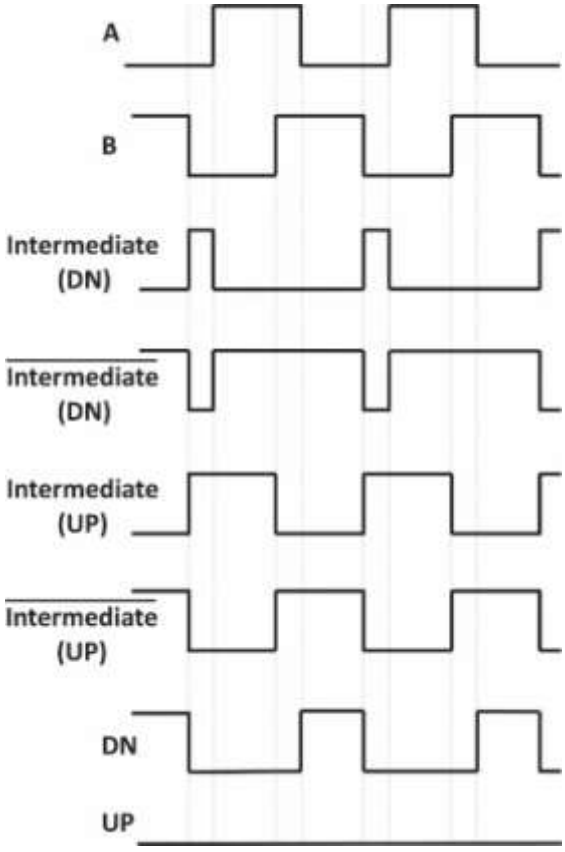

Figure 7. *UP and DN signal generation.*

The designed circuit is indicated in Figure 8. As can be seen, the UP signal zeroing can be delayed by applying delay on the intermediate signal path. The dead zone issue can be solved by this method. The dead zone in the DN signal can be omitted through the same method shown in Figure 8. b.

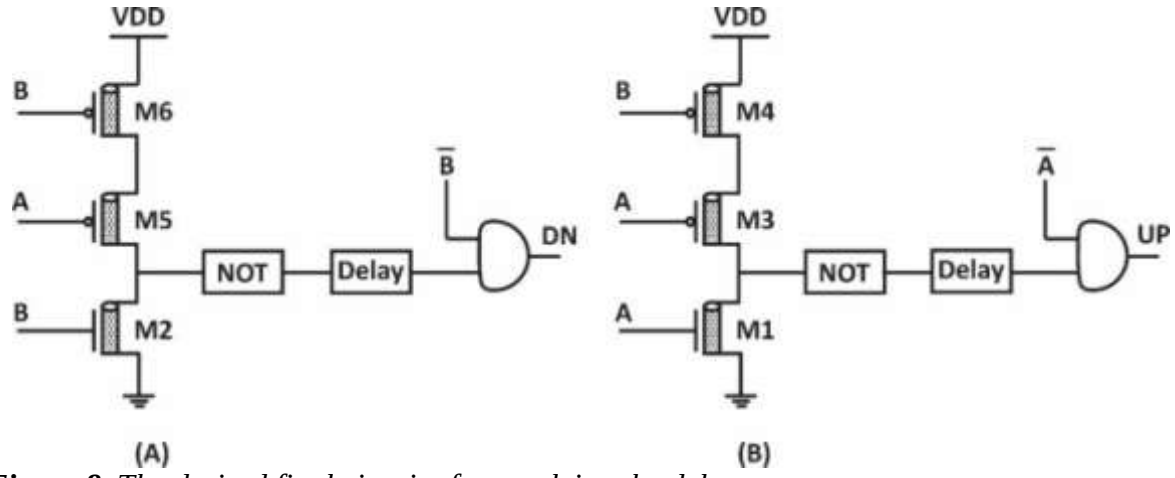

Figure 8. *The desired final circuit after applying the delay.*

The last signal after applying the delay can be seen in Figure 9. As can be seen, the dead zone can be entirely omitted by using this change. The situation in which B is ahead of A is also shown in Figure 10.

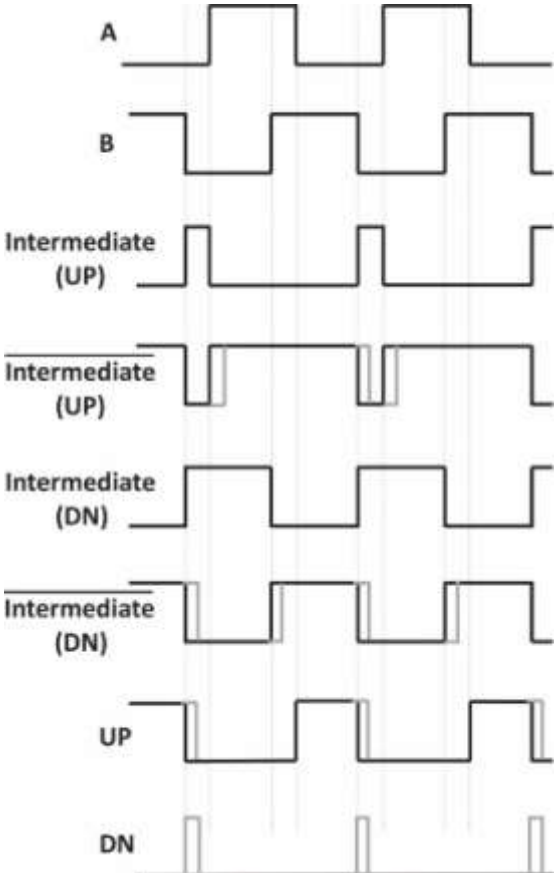

Figure 9. *Output signal circuit after applying the delay.*

The proposed circuit has a very low delay since, as seen in Figure 11, only path 2 is essential, and path 1 doesn't affect the delay. Therefore, the delay is only available in falling edge and includes delay in one AND gate. Therefore, since the proposed circuit has a simple structure, the speed of the circuit can be very high. Also, power consumption is sharply reduced due to omitting the rotational current.

The final proposed circuit is shown in Figure 12. The transistors are CNTFET, and Figure 13 shows the layout of the 180nm CMOS technology.

The symmetry of the proposed circuit regulates the path delays and reduces the leakage current. The occupation area of the proposed structure is 19×16 $(\mu m)^2$ and the total number of transistors are 22.

Nanotubes are actually layers of graphite that are joined at two points. The most important physical property of nanotubes is their electrical conductivity. The electrical conductivity of nanotubes varies from category to another category depending on the angle and type of bonds (chirality).

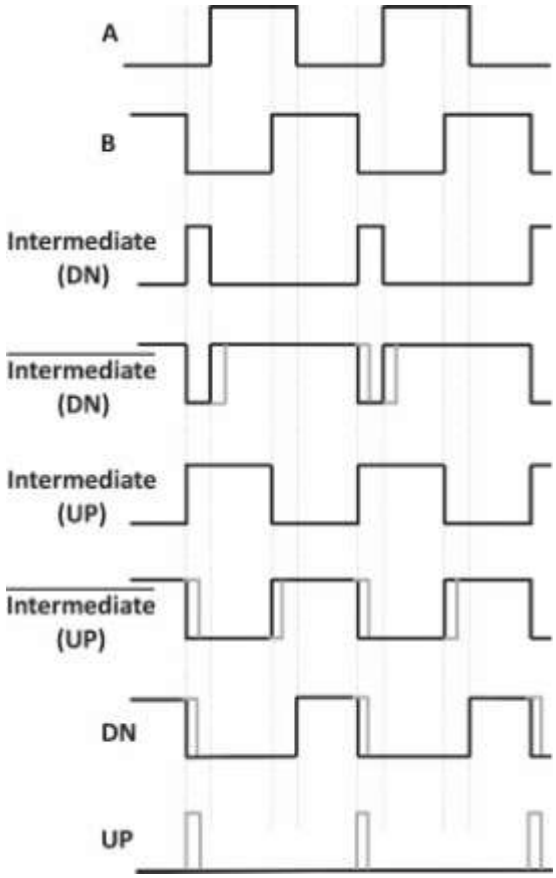

Figure 10. *Output signal circuit after applying the delay.*

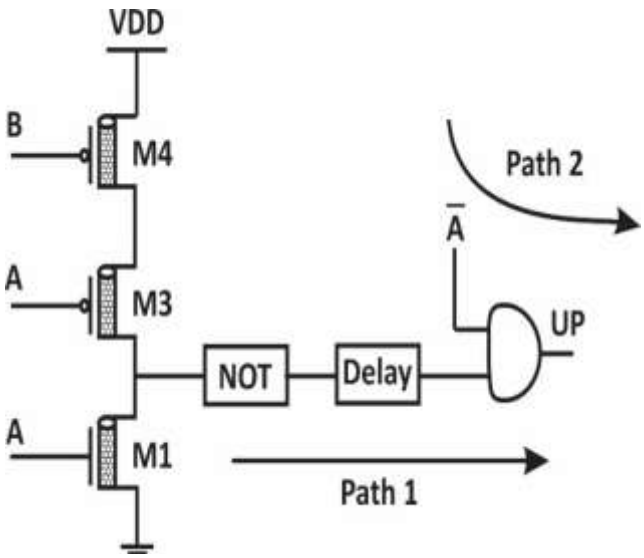

Figure 11. *Important paths in circuit's delay.*

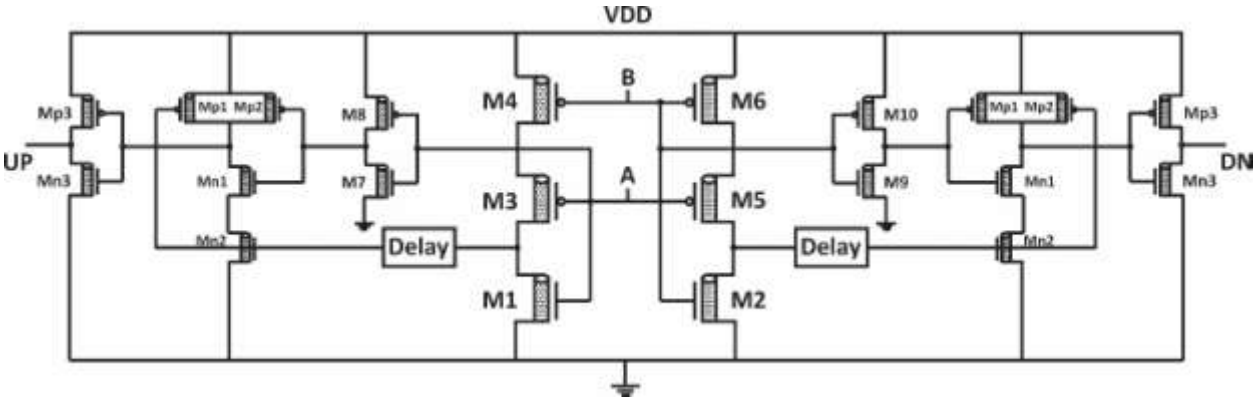

Figure 12. *Proposed PFD with CNTFET.*

Each atom is vibrating in its place. When an electron enters a set of atoms, the atoms vibrate and transmit the applied electric charge when they collide with each other. The classification is based on the order of the carbon atoms in the nanotubes and thus their conductivity. For example, the nanotube type of armchair is 1000 times more conductive than copper, while the zigzag type and the asymmetric type are semiconductor. The semiconductor properties of nanotubes vary depending on their type. Depending on the type of application, they are made in several categories.

The most important of them is Schottky barrier type, MOSFET-like and Dual-Gate CNTFET model. Due to the similarity of type, CMOS and CNTFET, in this paper, this type of transistor has been used to design the circuit.

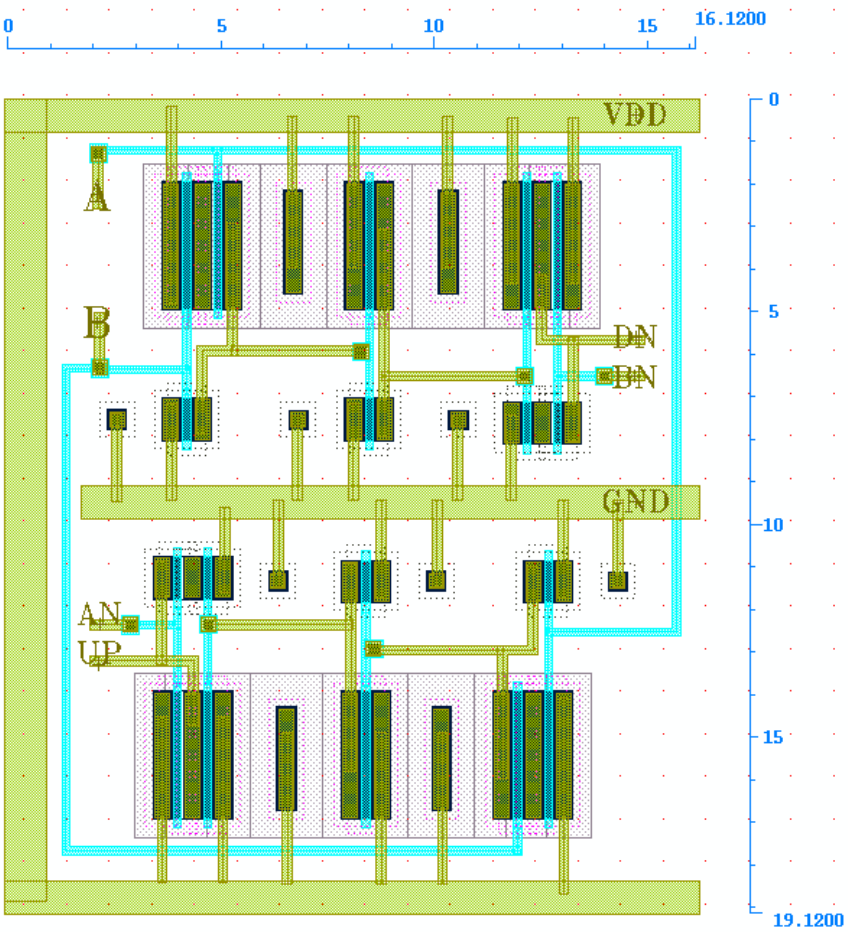

Figure 13. *Symmetric Layout of the proposed PFD.*

Equations (4) and (5) show how to calculate the threshold voltage for carbon nanotubes [17-21].

$$Vth = 0.42/(Dcnt(nm)) \quad (4)$$

$$Dcnt = \frac{a\sqrt{N_1{}^2 + N_2{}^2 + N_1N_2}}{\pi} \quad (5)$$

N_1 and N_2 determine the ratio of chirality that the two points on the graphene plate in the corners have (angles) to each other. Table 4 shows the threshold voltage of CNTFET for different chiralities.

Table 5 is the parameters used to simulate the proposed circuit:

Table 4. *Threshold voltage of CNTFET for different chiralities.*

Chirality (n1, n2)	D (nm)	Threshold Voltage (V)
(19, 0)	1.487	0.293
(10, 0)	0.783	0.557
(13, 0)	1.018	0.428

Table 5. *Threshold voltage of CNTFET for different chiralities [17].*

Chirality Type	Zigzag
Length of Channel	32 nm
Diameter	1.5 nm
Pitch	20 nm
K_{ox}	16
H_{ox}	4 nm

4. SIMULATION RESULTS

This circuit is simulated in Hspice software using the Stanford 32nm CNTFET technology model. The operational frequency is from 1 kHz to 20 GHz, with a power consumption of 1.76 μW in the highest operating frequency. Figure 14 indicates the simulation results using MATLAB. Axis x indicates the phase difference between two signals, and axis y indicates the difference between the average value of UP and DOWN signals. This PD is simulated in 1 GHz, 6 GHz, 12 GHz, and 18 GHz frequencies. The curve has to be linear in low-phase differences because nonlinearity causes a perturbation in the circuit. Still, the nonlinearity of these curves in high frequencies will not affect the circuit's performance because polarity is more important than magnitude.

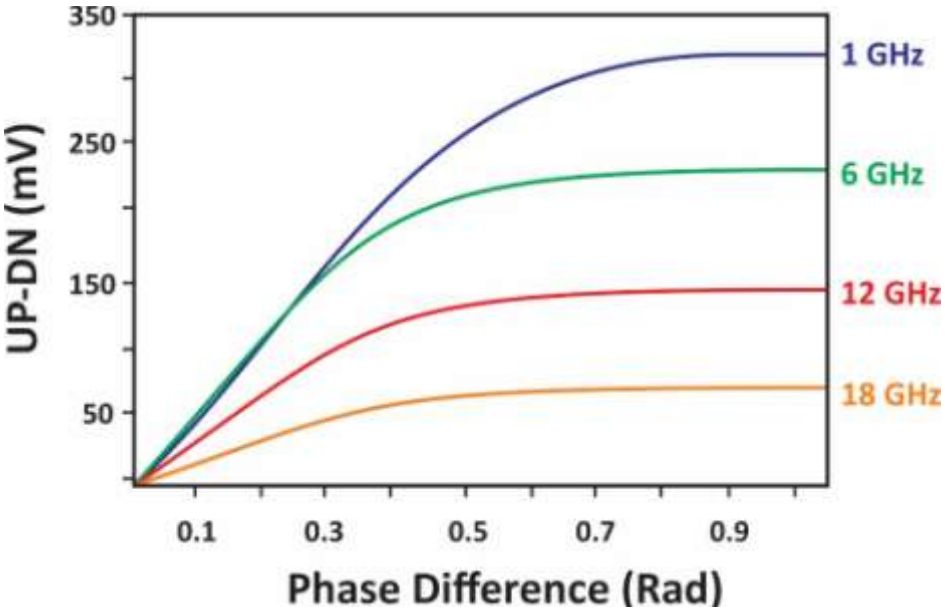

Figure 14. *Difference between average values of Up and Down signals versus the phase difference of two inputs.*

All of the UP and DN output waveforms related to this detector circuit are indicated in Figure 15 for when the "A" signal is leading compared to the "B" signal and for when the "A" signal is lagging compared to the "B" signal (Figure 16). The above circuit is also simulated in higher frequencies. Figure 17 indicates the waveforms related to the proposed detector in 20 GHz frequency using carbon nanotubes.

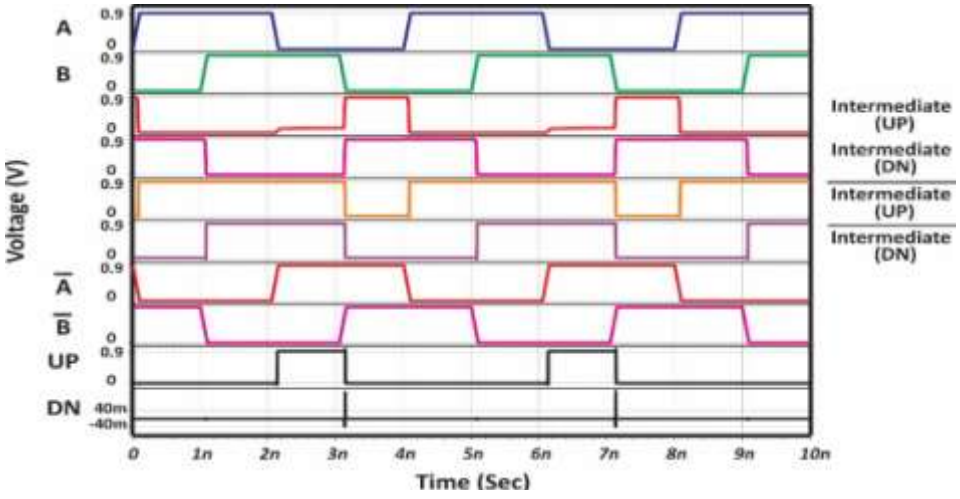

Figure 15. *Simulation results when "A" is in pre-phase situation.*

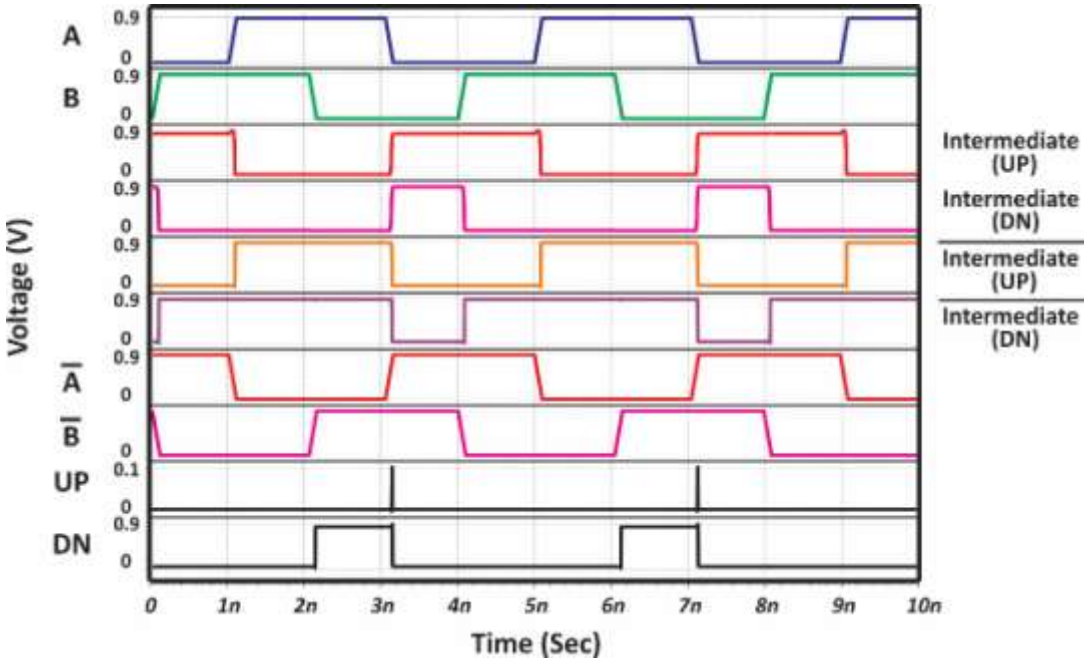

Figure 16. *Simulation results when "B" is in pre-phase situation.*

The output figure shows that the simulated results are identical to the analysis results. Figure 18 shows the simulation results when the inputs are in different frequencies.

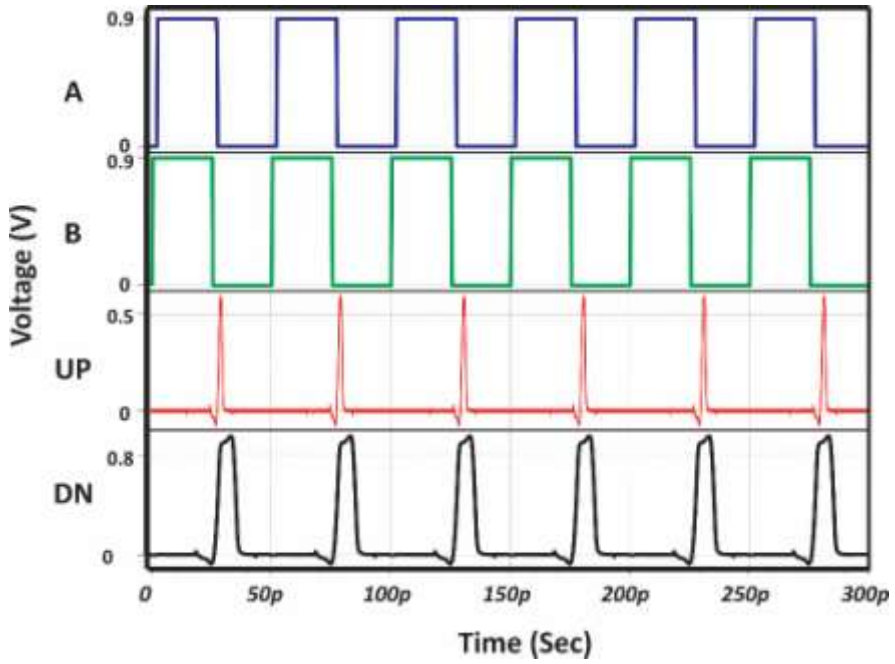

Figure 17. *Simulation results when the frequency is 20 GHz.*

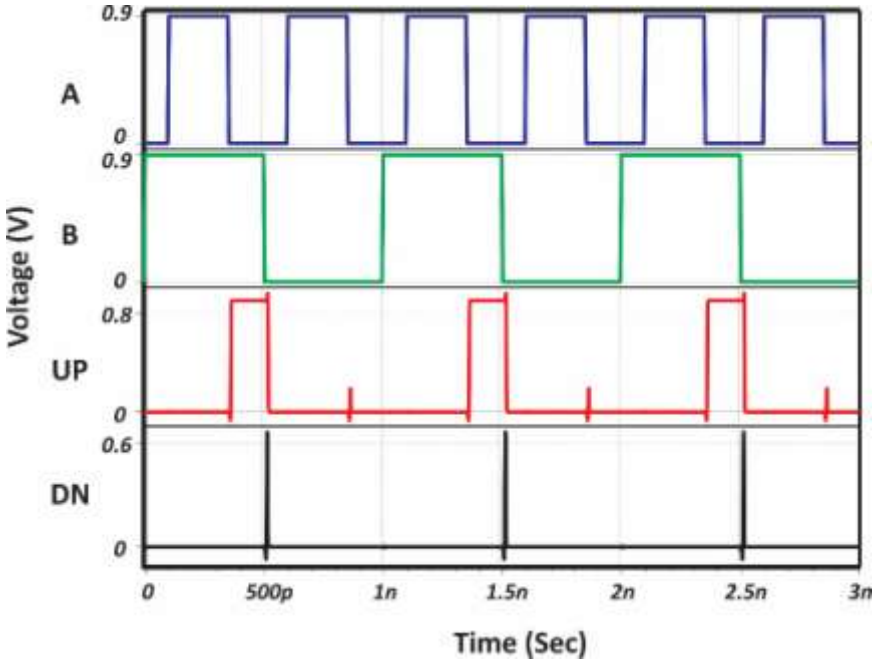

Figure 18. *Simulation results when the inputs are in different frequencies.*

As can be seen from the results, it's evident that the dead zone of the proposed phase detector circuit has a better situation than the conventional circuits in the same technology. Also, it's closer to the ideal situation. Essential parameters of this circuit, along with others, are presented in Table 6.

Table 6. *Comparison table with previous works.*

Reference	Max Freq. (Hz)	Power Cons. (Watt)	Ideal capture range	Supply (V)	Dead-Zone (S)	Reset Path	Tech. Type	No. of Transistors	Tech.
Conventional	1.1 G	780µ	4π	1.2	280p	Yes	CMOS	32	0.13 µm
[8]	3.44 G	324µ	4π	1.2	Free	Yes	CMOS	38	65 nm
[10]	3.8 G	285µ	4π	1.8	Free	No	CMOS	24	0.18 µm
[13]	3 G	134µ	4π	1.2	120p	Yes	CMOS	36	0.13 µm
[14]	2.5 G	NA	4π	1.2	0.75p	Yes	CMOS	>۴۰	90 nm
[15]	4.1 G	76µ	4π	1.2	25p	No	CMOS	20	0.13 µm
Proposed CMOS	4.2 G	120 µ	4π	1.2	Free	No	CMOS	28	0.18 µm
Proposed CNTFET	20 G	1.76 µ	4π	0.9	Free	No	CNTFET	28	32 nm

The review of the output parameters in the presence of different temperatures of the process is presented in Table 7, in which the output of the phase detector has undergone little change by applying changes in the presence of different threshold and temperature states, and its output is valid. The results indicate that the dead zone is reduced to zero, and the operation frequency was improved significantly compared to similar cases in CMOS and carbon nanotube transistors.

Table 7. *Results in different temperatures.*

Parameters	@ -40 ℃	@27 ℃	@80 ℃
Dead-Zone (ps)	Free	Free	Free
Max. Freq (GHz)	20.1	21.6	21.9
Power Consumption (μW)	176	1.36	0.9

In addition, the power consumption has its lowest possible value, and the results are valid even in 180 degrees phase difference.

5. Conclusion

In the new designs of the phase detector, the reset path has been removed, and the proposed circuit is an open loop so that the power consumption is lower and the lower dead zone can be reached. DFF-based phase detectors can have a lower operating frequency due to the DFF function. Therefore, this block has been removed in new designers to reach a higher working frequency. Next, the results show that removing the reset path and controlling the delays from input to output can achieve a shallow dead zone (close to zero). The proposed CMOS and CNTFET circuit, by injecting 30mV peak-to-peak power supply noise has 5 times the operating frequency of the conventional circuit, and it has a 10% improvement in power consumption of the conventional one by CMOS. Also, with carbon nanotubes, the frequency has increased 4 times, and the power consumption has improved significantly. In this case, the power consumption is 1.76 microwatts, and the operating frequency is 20 GHz.

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