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Analysis and Design of CNTFET-Based Electronic Circuits: A Review

Roberto Marani[1] and Anna Gina Perri[2,*]

[1]Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy, 70125, Bari, Italy
[2]Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, 70126, Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
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Abstract
In this review we present some design of CNTFET-based circuits, already proposed by us and here critically examined. For some of these, we compare the performance of proposed circuits both in CNTFET and CMOS technology. For CNTFET model, we use a compact, semi-empirical model, already proposed by us and briefly recalled, while, for the MOSFET model, we use the BSIM4 one of ADS library. Moreover in some design examples we compare our results with those obtained using the Stanford model. All simulations are carried out using the software ADS, which is compatible with the Verilog-A programming language.
Keywords: *CNTFET, CMOS, Modelling, Design of A/D circuits, Advanced Design System.*

1. INRODUCTION

We have been dealing with Carbon NanoTubes (CNTs) [1] and Carbon NanoTube Field Effect Transistors (CNTFETs) [2-11] for many years now. In particular we have studied extensively MOSFET-like CNTFET for high-performance and low-power memory designs [12-45].

In this review we present the design of CNTFET-based circuits, already proposed by us and here critically examined.

For some of these, we compare the performance of proposed circuits both in CNTFET and CMOS technology.

For CNTFET model, we use a compact, semi-empirical model, already proposed by us [2-3] and briefly recalled, while, for the MOSFET model, we use the BSIM4 one of ADS library. BSIM (Berkeley Short-channel IGFET Model) [46] refers to a family of MOSFETs for integrated circuit design.

Moreover in some design examples we compare our results with those obtained using the Stanford model [47-50].

All simulations are carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [51].

The presentation is organized as follows.

Section 2 gives a brief review of CNTFET and MOSFET models used.

Then in Sections 3 and 4 respectively we review the performances of a common source and of common drain amplifier realized both with a CNTFET and then with a MOSFET.

In Section 5 we critically review the design of a CNTFET differential amplifier, proposing a comparative analysis of CNTFET models, while a full adder circuit design in CNTFET and CMOS technology are examined in Section 6.

Finally Section 7 gives the conclusions and future developments.

2. A BRIEF REVIEW OF CNTFET AND MOSFET MODELS

An exhaustive description of our CNTFET model is in [2-3] and therefore the reader is requested to consult them.

The model, based on the hypothesis of ballistic transport, makes reference to [52] and on the following improvements introduced in [53-54] to solve some numerical problems of the original paper [52].

In this Section we just describe the main equations on which our I-V model is based.

When a positive voltage is applied between drain-source ($V_{DS} > 0$ V), the hypothesis of ballistic transport[3] allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source ($V_{GS} > 0$ V), the conduction band at the channel beginning decreases by qV_{CNT}, where V_{CNT} is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [55]:

$$I_{DSp} = \frac{4qkT}{h}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, ξ_{Sp} and ξ_{Dp} have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT}$$

$$\xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \quad (2)$$

being E_{Cp} the sub-bands conduction minima.

Therefore the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (3)$$

The surface potential, V_{CNT}, is evaluated by the following approximation [2]:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \frac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \frac{E_C}{q}\right) & \text{for } V_{GS} \geq \frac{E_C}{q} \end{cases} \quad (4)$$

where E_C is the conduction band minima for the first sub-band.

The parameter α depends on V_{DS} voltage, CNTFET diameter and gate oxide capacitance C_{ox} [2-3].

Regarding the C-V model, an exhaustive description of our C-V model is widely described in [7-8] and therefore the reader is requested to consult these references, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are widely explained:

$$\begin{cases} C_{GD} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (5)$$

In order to simulate correctly the CNTFET behavior, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

We have achieved this goal using an empirical method exhaustively described in [2-3], where we explained that V_{FB}, R_D, R_S have been determined by a best-fit procedure between the measured and simulated values of I-V characteristics of the device, while the quantum capacitances have been computed from the charge in the channel.

In this way all elements of the CNTFET equivalent circuit are determined.

Figure 1 shows our model, in which we have reported the values of circuital elements.

It is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{drain} and L_{source} and the resistances R_{drain}

and R_{source}, in which the parasitic effect due to the electrodes are also included.

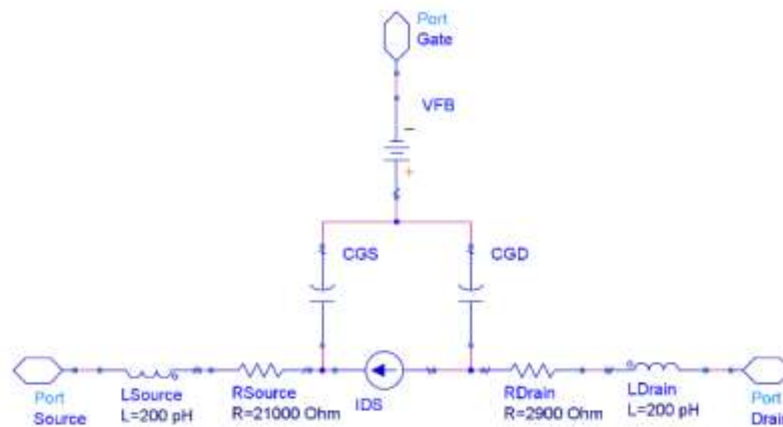


Figure 1. *Equivalent circuit of an n-type CNTFET.*

Other authors [56-57] have then assumed these parameters fixed to constant and typical values (i.e. V_{FB} = 0 V [56] and $R_D = R_S$ = 25 kΩ [57]), thus losing the dependence on the CNT diameter.

Regards to the CNT quantum inductance, as shown in Figure 1, we have assumed constant and equal to 4 pH/nm, which we have splitted up into two inductances of 2 pH/nm, while the classical self-inductance, as it is known [56], can be ignored.

As already said, for the MOSFET model we use the BSIM4 model of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [46] refers to a family of MOSFETs for integrated circuit design. In this work BSIM4 has been used for the 32 nm technology nodes. The MOSFET parameters for BSIM4 model were obtained by Predictive Technology Model (PTM) web site from the Nanoscale Integration and Modelling Group of Arizona State University. In particular the MOSFET parameters, obtained using an evolution of previous Berkeley Predictive Technology Model (BPTM), have been improved by us through parametric simulations to obtain performance of the MOSFET model comparable to the CNTFET one. As in some design examples we will compare our results with those obtained using the Stanford model [49-50], we also make a brief recall of this model,

The Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET) is a semi-empirical model that describes the current-voltage (I-V) and capacitance-voltage (C-V) characteristics in a short-channel metal-oxide-semi-conductor field-effect transistor (MOSFET) with carbon nanotubes as the channel material. In particular the VS-CNFET model is based on the semi-empirical virtual source concept calibrated to experimental data. The intrinsic drain current and terminal charges are based on the virtual source (VS) model, with the virtual source velocity extracted from experimental data for different channel lengths (ranging from 3-um down to 15-nm). Moreover, the VS-CNFET model takes to account the following parasitic effects:

1. direct source-to-drain and band-to-band tunnelling current calibrated by numerical simulations;
2. metal-to-CNT contact resistances calibrated by experimental data;
3. parasitic capacitance including gate-to-CNT fringe capacitances and gate-to-contact coupling capacitances.

The inputs to the VS-CNFET model are the physical device design including device dimensions, CNT diameter, gate oxide thickness, etc.

3. DESIGN OF A COMMON SOURCE AMPLIFIER IN CNTFET AND MOSFET TECHNOLOGY

In this section we review the performances of a common source (C-S) amplifier realized both with a CNTFET and then with a MOSFET. The circuital configurations are shown in Figures 2 and 3 respectively.

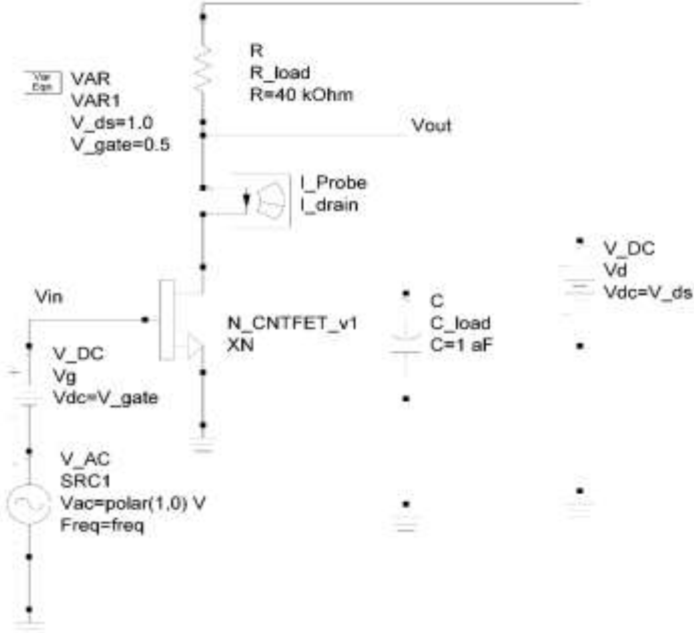


Figure 2. *C-S amplifier based on CNTFET.*

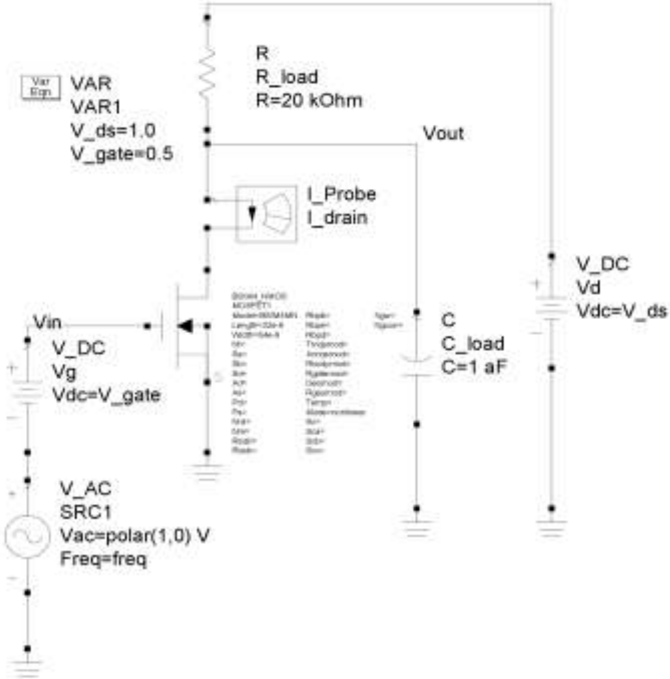


Figure 3*. C-S amplifier with MOSFET in 32 nm technology.*

We have used a C_load =1 aF for both amplifiers and a different value for R_load (40 KΩ for CNTFET and 20 KΩ for MOSFET) in order to have comparable

results, because the intrinsic parameters of the two active devices are different.

In particular we compare the values obtained from the simulations with those obtained by theoretical calculation using the following formulas [58]:

$$A_V = -g_m \frac{r_o R_D}{r_o + R_D}$$

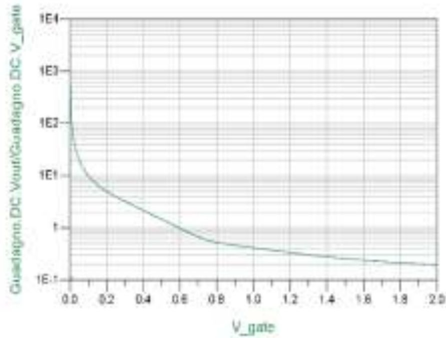
$$R_{OUT} = \frac{r_o R_D}{r_o + R_D} \qquad (6)$$

As the gate is isolated, the input resistance of the stage is infinite ($R_{IN} \cong \infty$). Moreover $R_D = R_{LOAD}$. The analysis of the previous circuits have been obtained used the parameters reported in Table 1.

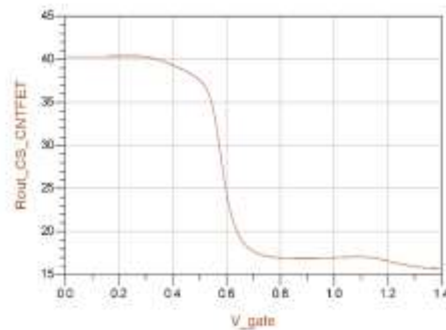
Table 1. *Parameter values.*

Device	V_G	V_D	I_D	g_m	r_o
MOSFET 32nm	0.5 V	1V	16.3 μA	0.178 mA/V	9.6 kΩ
CNTFET	0.5 V	1V	6.8 μA	0.035 mA/V	200 kΩ

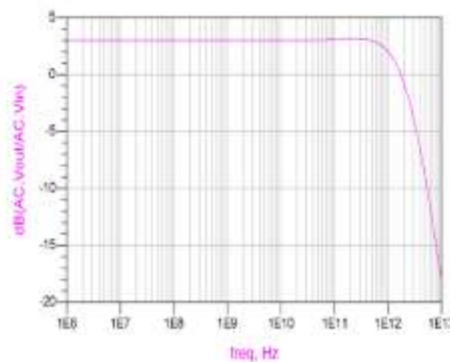
The simulations results are shown in Figures 4 and 5. In Table 2 we compare the values obtained from the simulations with those obtained by theoretical calculations [58].



(a)

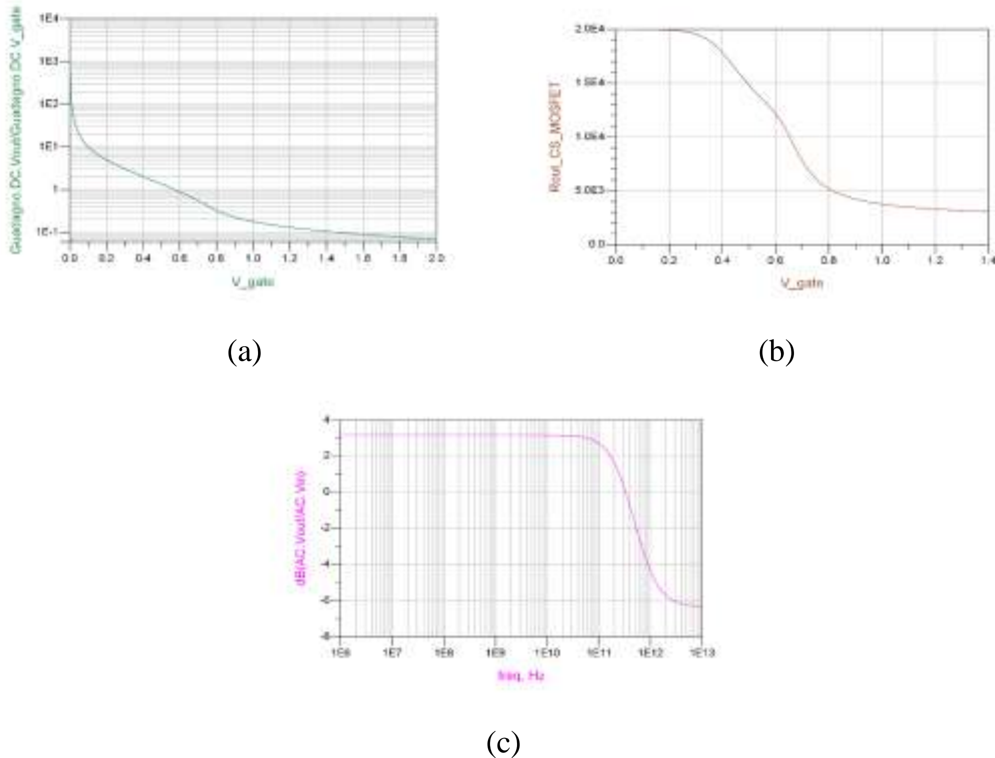


(b)



(c)

Figure 4*. Simulation results for the C-S amplifier with CNTFET: (a) voltage gain; (b) output resistance; (c) frequency response.*



(a) (b)

(c)

***Figure 5**. Simulation results for the C-S amplifier with 32 nm MOSFET: (a) voltage gain; (b) output resistance; (c) frequency response.*

***Table 2.** Theoretical and simulated values of A_V and R_{OUT}.*

	MOSFET 32 nm		CNTFET	
	THEORETICAL VALUES	SIMULATED VALUES	THEORETICAL VALUES	SIMULATED VALUES
A_V	- 1.15	- 1.48	- 1.16	- 1.41
R_{OUT}	6.48 kΩ	14.35 kΩ	33.34 kΩ	37.45 kΩ

It is clear that the use of a CNTFET rather than a MOSFET improves the performance of a common source amplifier. In fact, for equal gains, there is a halving of the current and a widening of the pass band of about 1.2 THz, being the MOSFET cut-off frequency f_c = 316 GHz and the CNTFET cut-off frequency f_c = 1.5 THz, as you can be easily seen by analyzing the Figures 4c and 5c respectively.

4. DESIGN OF A COMMON DRAIN AMPLIFIER IN CNTFET AND MOSFET TECHNOLOGY

In this section we review the performances of a common drain (C-D) amplifier realized both with a CNTFET and then with a MOSFET. In particular we compared the values obtained from the simulations with those obtained by theoretical calculation using the following formulas [58]:

$$A_V = \frac{g_m (r_o // R_S)}{1 + g_m (r_o // R_S)} \quad (7)$$

$$R_{OUT} = r_o // R_S // \left(\frac{1}{g_m}\right) \quad (8)$$

Also in this case, as the gate is isolated, the input resistance of the stage is infinite ($R_{IN} \cong \infty$). Moreover $R_S = R_{LOAD}$.

The analysis have been obtained used the parameters reported in Table 3.

Table 3. *Parameter values.*

Device	V_G	V_D	I_D	g_m	r_o
MOSFET 32 nm	1.5 V	3V	1.45 µA	0.053 mA/V	9.6 kΩ
CNTFET	1.5 V	3V	1.18 µA	0.035 mA/V	200 kΩ

The design technique is the same previously examined for a C-S amplifier and therefore, in order to avoid overloading the discussion, we limit ourselves to report in Table 4 the values obtained from the simulations with those obtained by theoretical calculations [58].

Table 4. *Theoretical and simulated values of A_V and R_{OUT}.*

	MOSFET 32 nm		CNTFET	
	THEORETICAL VALUES	SIMULATED VALUES	THEORETICAL VALUES	SIMULATED VALUES
A_V	0.34	0.66	0.85	0.79
R_{OUT}	6.2 kΩ	1.7 kΩ	24 kΩ	21.6 kΩ

It is useful to point out that in the theoretical calculations made for the MOSFET configuration, it was possible to neglect the source resistance (R_S = 1000 KΩ) in parallel with the MOSFET output resistance (r_o = 9.6 KΩ) being R_S much greater than r_o. Moreover, also for a C-D amplifier we have a pass band of 525 GHz for MOSFET configuration and 14.4 THz for CNTFET configuration.

5. DESIGN OF A DIFFERENTIAL AMPLIFIER: COMPARATIVE ANALYSIS OF CNTFET MODELS

In Figure 6 we show a differential amplifier with symmetric supplies, the positive V_{DD} = 2 V the negative -V_{DD} = -2V (named MinusVDD [33].

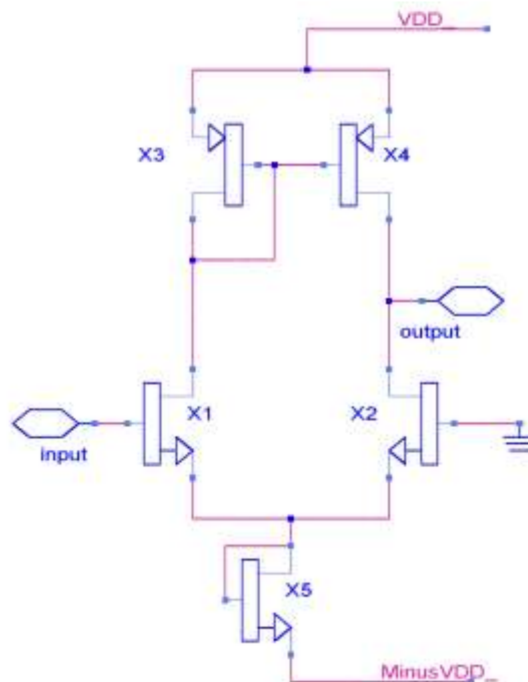


Figure 6. *Differential circuit using CNTFET.*

We use five CNTFET, X1 X2 X3 X4 X5, each made by a single carbon nanotube channel with indices (19,0) and length 25 nm.

These values derive from a previous analysis [41], where we observed that short tubes gives the best performance at high frequency. In order to simulate the output load, both drain of the differential pair are directly coupled to gate input of a differential pair complementary to the one in Figure 6, i.e. obtained swapping position of differential pair and a current generator, and swapping N devices with P devices.

We ignore the embedding parasitic element, since these would cut down the gain at higher frequencies and cover differences between models.

As the Stanford model includes voltage independent capacitances, presumably for terminal pads, we measured values of these capacitances from simulation of a bare CNTFET obtaining a 2.19 aF capacitance between gate and source, and a 1.44 aF capacitance between drain an source.

To make comparison more balanced we add two capacitor to our model with these values. We consider first the polarizations: in Figure 7 we show the drain current of the differential pair, our model foresees lower current, from 30% less at $V_{DD} = 1$ V to 15% less at $V_{DD} = 2$ V.

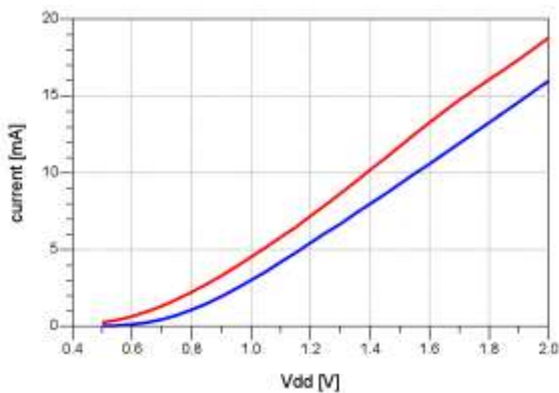


Figure 7. Drain current of differential pair of Figure 6, for various supply voltages. The blue line represent our model results and the red line the Stanford model results.

V_{ds} for the differential pair is lower, while the V_{ds} of the current source is higher, the difference being about 0.1V.

In Figure 8 the differential voltage gain of the proposed circuit at low frequencies, below 1 GHz, foreseen by our model is 21.2 dB, while Stanford model is 0.7 dB lower.

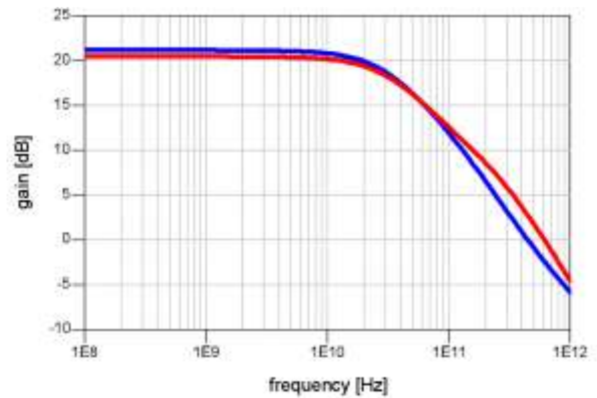


Figure 8. Differential gain. Colours as for Figure 7.

For the 3 dB cut frequencies, values are 34 GHz for our model and 12% higher, 38 GHz, for Stanford model. On the tail of the curve, the 0 dB gain frequency is 0.44 THz for our model and 36% higher, 0.60 THz for Stanford model.

In Figure 9 we show the transient analysis for an input differential sine of V_{in} =±1 mV amplitude at 50 GHz, at a frequency above the 3 dB cut frequency since linear simulation foresee 6.57 (16 dB) voltage gain.

Transient simulation shows a small transient in the form of decreasing exponential, which appears as a slow derive of the mean voltage of the signal, its voltage values at first peak of sinusoid is 1.0 mV for our model and 0.8 mV for Stanford one. Distortion is not negligible and not visible in Figure 9 since input signal amplitude is small compared to the harmonic intercept value, that we will show later.

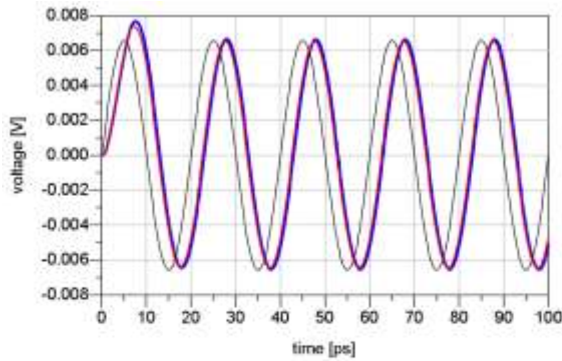


***Figure 9**. Transient output for sinusoidal input. The input differential signal is in black, the output is in blue for our model and in red for Stanford model. Input has been multiplied by the gain obtained from linear analysis using our model. Continuous components have been subtracted.*

We present in Figure 10 the differential input admittance, while in Figure 11 the output single ended impedance.

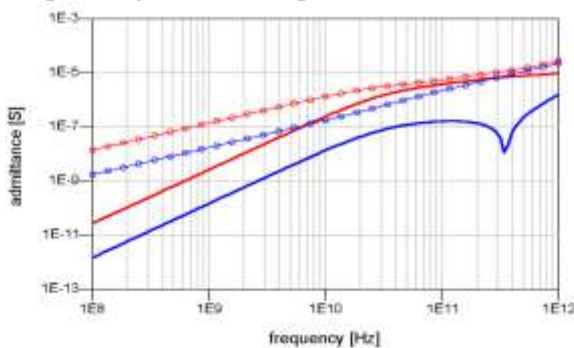


***Figure 10**. Differential input admittance, continuous line are real part, while imaginary parts is represented with a line plus circles. Colours as for Figure 7.*

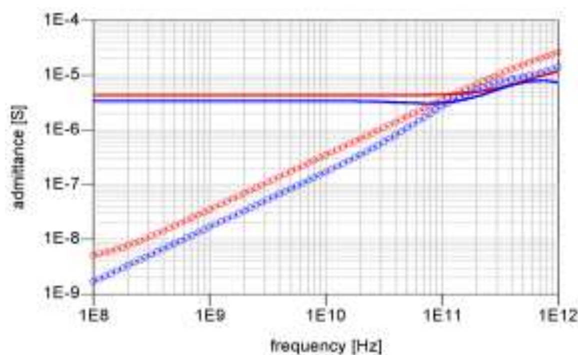


***Figure 11**. Output impedance, continuous line are for the real part, circles for imaginary part. Colours as for Figure 7.*

The input differential admittance is dominated by a capacitance component, our model foresees a value 8 times smaller than the values from Stanford model for frequencies below 100 GHz

For the output impedance, the resistive component is dominant at frequencies below 100 GHz, above this frequency the capacitive component became dominant. For frequencies below 100 GHz our model foresee 20% lower real part and 50% lower capacitive part, above this frequency, our model still gives lower result but relative differences depends on frequency.

Regards to harmonic distortion, we made a transient simulation with a differential input signal at 50 GHz, measuring the simulated output harmonic component for various periods until we see transient effects disappear. Since transient effect are detectable till the 5th period, we selected the 40th period to measure the harmonic components from 2nd to the 5th.

In Table 5 we list the ratios of higher harmonic to the first harmonic.

The values for the k-th harmonic distortion relative to the first harmonic could be easily approximated with the function $(V_{in}/V_k)^{k-1}$ from which we could obtain the values of the intercept V_k, that we present in Table 6.

We observe that obtained values for V_k are almost independent from V_{in} as it should be.

Since we have to seek for the lowest V_k value, from Table 6 we obtain an intercept at 25mV for our model, and at 27mV for Stanford model, in both cases due to the 5th harmonic.

If we use Table 5 to compare distortion values, we observe that the worst case is the 3rd harmonic distortion for which our model foresee a distortion 2.30 times that foreseen by Stanford model. For the other harmonics the difference is smaller but our model still predicts larger distortions. We stress that none of the examined model consider self-heating due to power dissipation.

Table 5. *Ratio of the higher harmonic to the fundamental component at 50 GHz. Unreported values are covered by numerical noise.*

V_{in}	Harmonics (our model)				Harmonics (Stanford model)			
[V]	2nd	3rd	4th	5th	2nd	3rd	4th	5th
10^{-3}	$1.38\ 10^{-2}$	$1.15\ 10^{-3}$	$5.40\ 10^{-5}$	$2.00\ 10^{-6}$	$9.31\ 10^{-3}$	$4.49\ 10^{-4}$	$3.05\ 10^{-5}$	$1.90\ 10^{-6}$
10^{-4}	$1.38\ 10^{-3}$	$1.15\ 10^{-5}$	$5.40\ 10^{-8}$	$2.66\ 10^{-10}$	$9.22\ 10^{-4}$	$4.41\ 10^{-4}$	$2.97\ 10^{-8}$	$1.85\ 10^{-10}$
10^{-5}	$1.38\ 10^{-4}$	-	-	-	$9.22\ 10^{-5}$	$4.41\ 10^{-4}$	$3.00\ 10^{-11}$	-
10^{-6}	$1.38\ 10^{-5}$	-	-	-	$9.21\ 10^{-6}$	-	-	-

Table 6. *Intercept point for harmonic components at 50 GHz obtained by Table 5.*

V_{in}	Harmonics intercept (our model)				Harmonics intercept (Stanford model)			
	2nd	3rd	4th	5th	2nd	3rd	4th	5th
[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]
10^{-3}	0.0727	0.0295	0.0265	0.0266	0.1074	0.0472	0.0320	0.027
10^{-4}	0.0725	0.0295	0.0264	0.0248	0.1085	0.0476	0.0323	0.027
10^{-5}	0.0725	-	-	-	0.1085	0.0476	0.0322	-
10^{-6}	0.0725	-	-	-	0.1085	-	-	-

Definitely the values of gain, between the two considered models, at various frequencies are comparable, with comparable results for characteristic frequency point at − 3 dB and at gain = 1. The largest difference between the simulation results comes from the differential input admittance for which our model foresees a value 8 times smaller.

For distortions, while our model predicts always higher values for harmonic distortions, we obtained similar results for the harmonic intercept since this value is due to the 5th harmonic for which models predict similar results.

6. FULL ADDER CIRCUIT DESIGN IN CNTFET AND CMOS TECHNOLOGY

A Full Adder [58] adds binary numbers and has three inputs and two outputs. The two inputs are A and B, and the third input is a carry input C_{IN}. The output carry is designated as C_{OUT}, and the normal output is designated as S_{UM}.

The truth table of the full adder circuit is shown in Table 7.

Table 7. *Truth table of a Full Adder.*

A	B	C_{IN}	C_{OUT}	S_{UM}
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The circuit of Figure 12 realizes the function proposed by truth table, where XOR gate is realized with NAND gates, as the schematic of Figure 13.

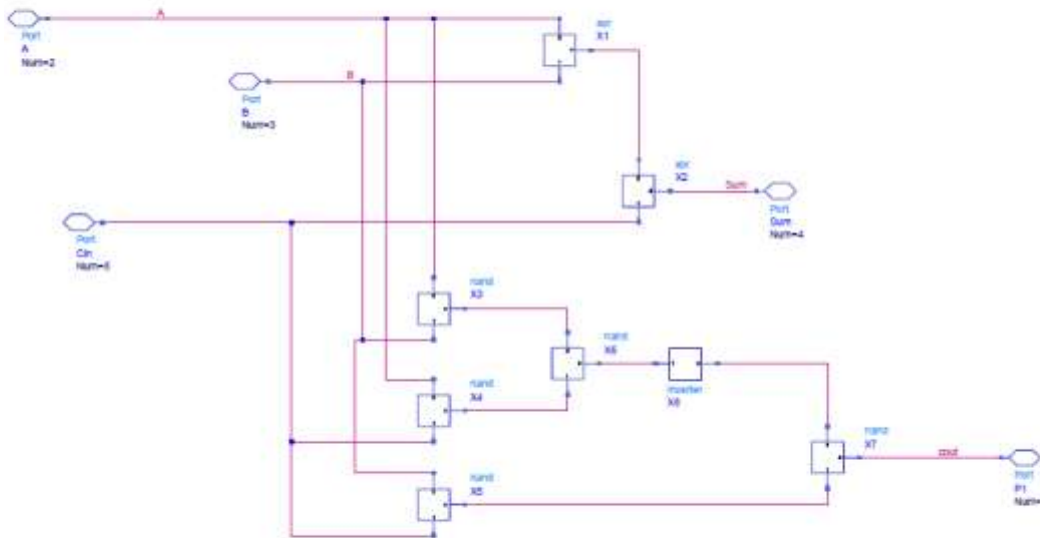


***Figure 12**. Full adder schematic.*

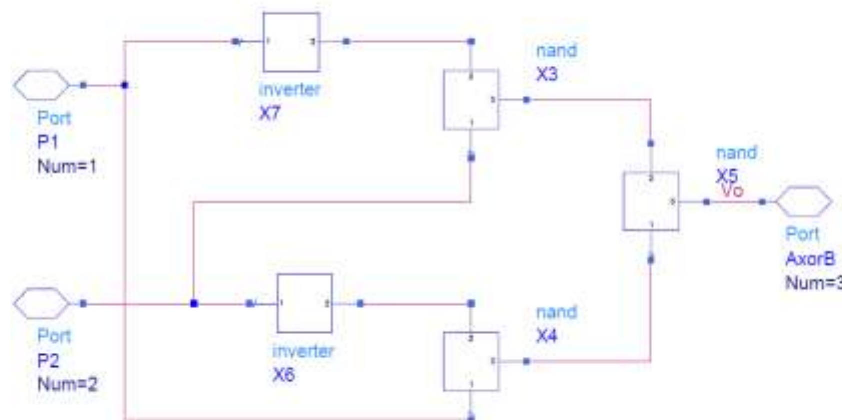


***Figure 13**. XOR schematic.*

The simulations to verify the correct mode of operation of the proposed full adder (realized using NAND and NOT gates) in CNTFET technology, have been made, doing compromise choice.

As we have widely illustrated in [36], for a supply voltage of 0.5 V the NAND and NOT gates present a Voltage Transfer Characteristics (VTC), that allows the correct mode of operation because there is a clear division between the high logic state and the low logic state. Therefore we have fixed a supply voltage of 0.5 V.

Assuming Cin = 1 for all simulations, Figures 14, 15, 16 and 17 show output and input signals of the full adder at 1 GHz, 30 GHz, 50 GHz and 80 GHz, respectively.

From the analysis of the previous figures, we can affirm that the limit for a correct mode of operation is 50 GHz. In fact, with a frequency of 80 GHz (Figure 17), the output S_{UM} completely loses its meaning.

Regards to a full adder in CMOS technology, in [37] we have illustrated that for a supply voltage of 3 V the NAND and NOT gates present a VTC that allows the correct mode of operation because there is a better frequency characteristic. Therefore we have fixed a supply voltage of 3 V.

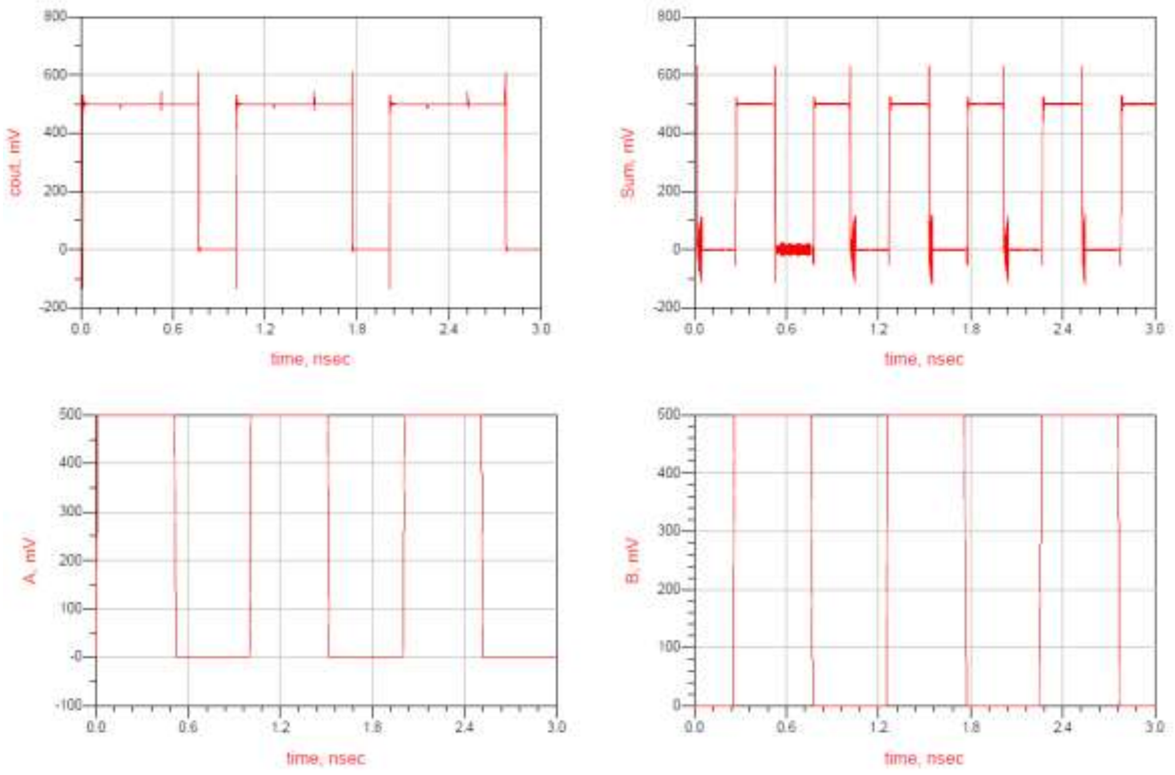


***Figure 14**. Output and input signals of the full adder at 1 GHz.*

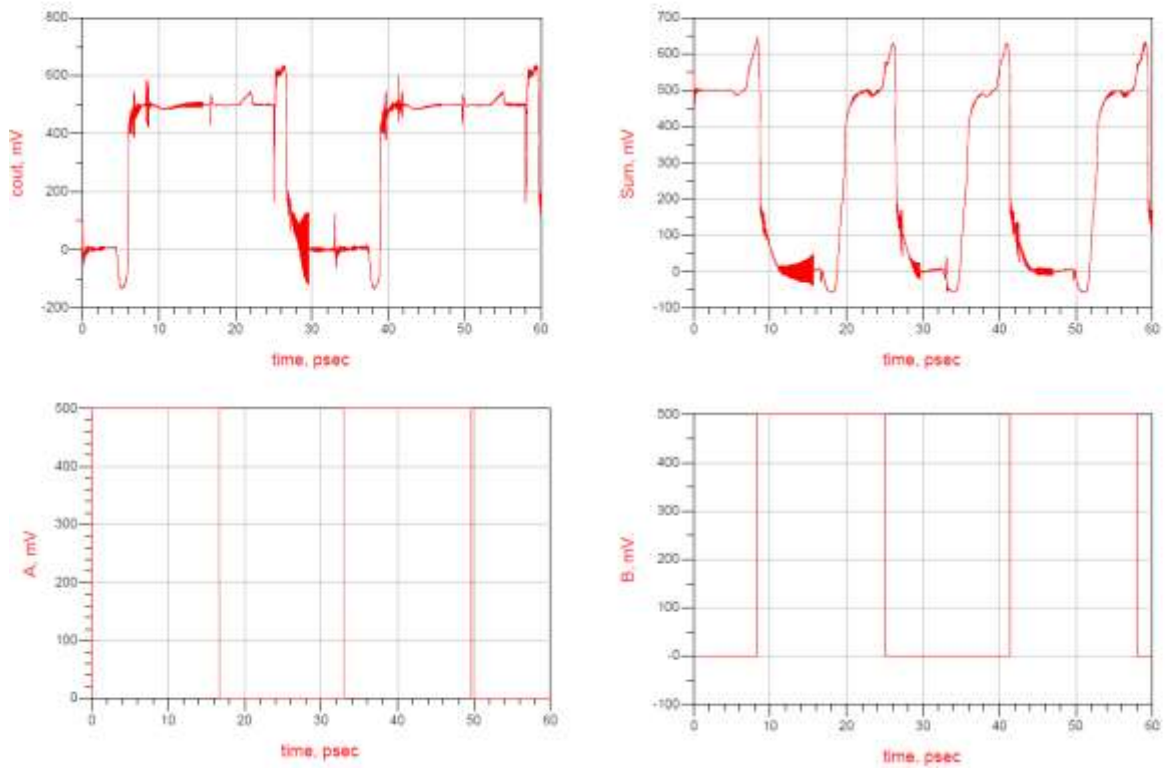


***Figure 15**. Output and input signals at 30 GHz.*

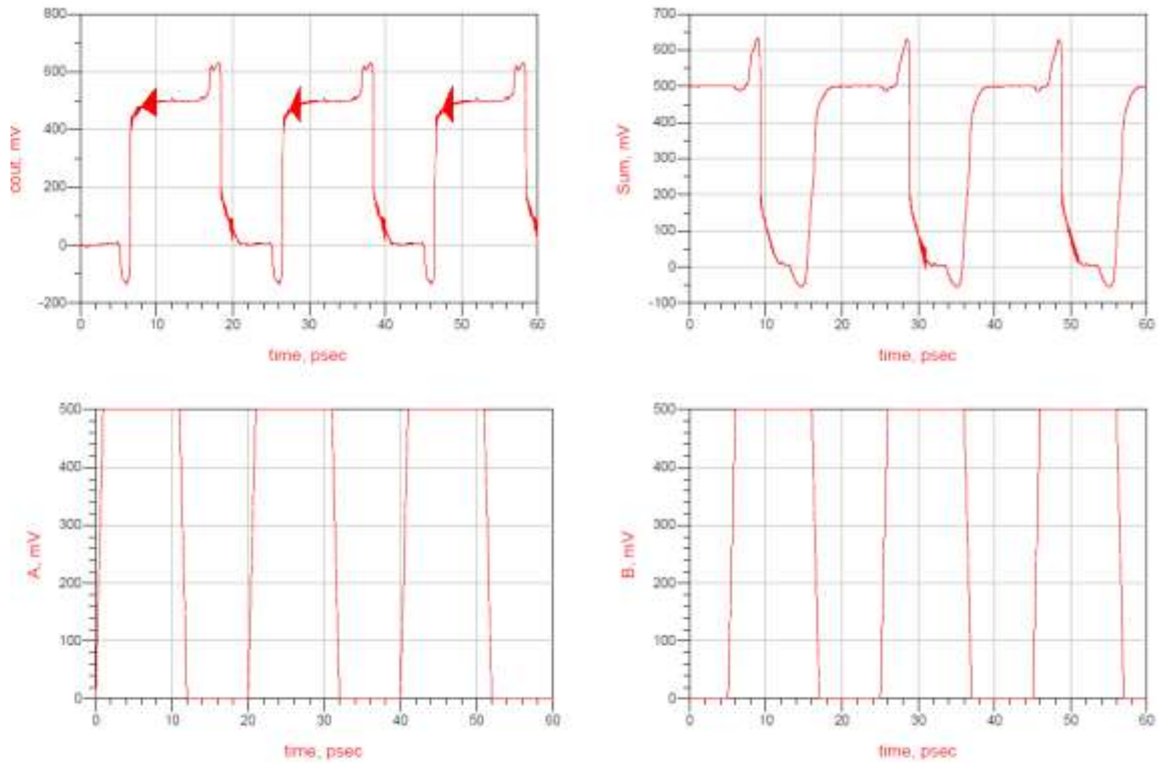


***Figure 16**. Output and input signals at 50 GHz.*

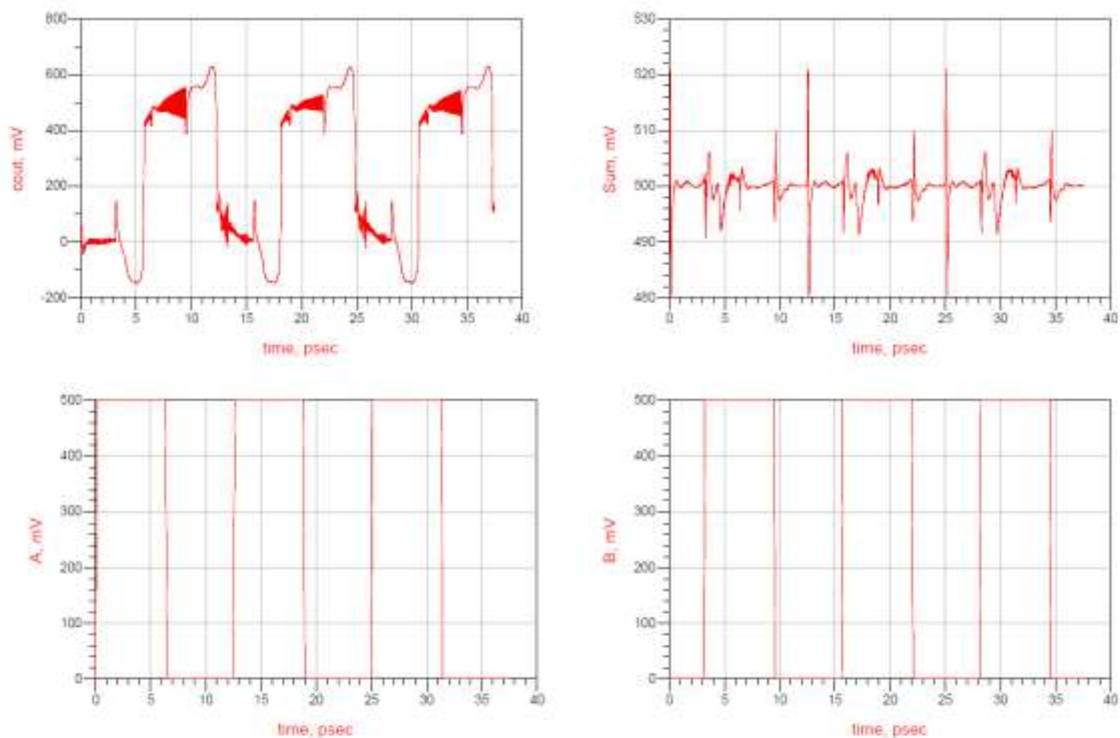


***Figure 17**. Output and input signals at 80 GHz.*

In order not to burden the discussion, we limit ourselves to reporting the final results of the simulations, already shown in [37].

In this case the limit for a correct mode of operation is 200 MHz. In fact with a frequency of 333 MHz the output S_{UM} completely loses its meaning.

Finally, in Table 8 we show the obtained results for power delay product (PDP), frequency and propagation delay for a NOT gate both in CNTFET and in CMOS technology, in order to compare the two technologies.

It is possible observe that the CNTFET logic family uses less energy than CMOS for to do a commutation of the output. Moreover CNTFETs devices are quicker than CMOS, having less time delay and greater work frequency, and the low voltage supply allows the use of CNTFET for low power applications.

Table 8. *Comparison between CNTFET and CMOS technology (NOT gate).*

Obtained values	CNTFET	CMOS
Power delay product (J)	$3.32 \cdot 10^{-18}$	$5.8 \cdot 10^{-13}$
Work frequency (Hz)	$50 \cdot 10^{9}$	$200 \cdot 10^{6}$
Propagation delay t_P (s)	$1.52 \cdot 10^{-12}$	$2.5 \cdot 10^{-10}$
V_{dd} (V)	0.5	3

7. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this review we presented some design of CNTFET-based circuits, already proposed by us and here critically examined.

For some of these, we compared the performance of proposed circuits both in CNTFET and CMOS technology.

For CNTFET model, we used a compact, semi-empirical model, already proposed by us and briefly recalled, while, for MOSFET model, we used the BSIM4 one of ADS library.

For C-S and C-D amplifier and Full Adder design we compared the performance of circuits both in CNTFET and CMOS technology, highlighting the differences between the two technologies.

In particular we shown that the use of a CNTFET rather than a MOSFET improves the performance of a common source amplifier. In fact the CNTFET cut-off frequency f_c is 1.5 THz, while the MOSFET one is 316 GHz. Moreover, for a C-D amplifier we have obtained a pass band of 525 GHz for MOSFET configuration and 14.4 THz for CNTFET configuration.

Regards to the Full Adder design, we demonstrated that the CNTFET logic family uses less energy than CMOS for to do a commutation of the output. Moreover CNTFETs devices are quicker than CMOS, having less time delay and greater work frequency, and the low voltage supply allows the use of CNTFET for low power applications.

For differential amplifier design we have compared our results with those obtained using the Stanford model. Also in this case we quantitatively highlighted the differences between the two models.

All simulations have been carried out using the software ADS.

Currently we are working to study the effect of temperature and of noise in other circuits based on CNTFETs.

Moreover we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits and the impact of technology on CNTFET-based circuits performance.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. Marani, R., Perri, A. G., "CNTFET Modelling for Electronic Circuit Design", *ElectroChemical Transactions*, 23 (2009) 429-437.
2. Gelao, G., Marani, R., Diana, R., Perri, A. G., "A Semi-Empirical SPICE Model for *n*-type Conventional CNTFETs", *IEEE Transactions on Nanotechnology*, 10 (2011) 506-512.

3. Marani, R., Perri, A. G., "A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software", *Current Nanoscience*, 7 (2011) 245-253.
4. Marani, R., Perri, A. G., "A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications", *International Journal of Electronics*, 99 (2012) 427-444.
5. Marani, R., Gelao, G., Perri, A. G., "Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation", *Current Nanoscience*, 8 (2012) 556-565.
6. Marani, R., Gelao, G., Perri, A. G., "Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design", *Microelectronics Journal*, 44 (2013) 33-39.
7. Marani, R., Perri, A.G., "Modelling of CNTFETs for Computer Aided Design of A/D Electronic Circuits", *Current Nanoscience*, 10 (2014) 326-333.
8. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis", *Current Nanoscience*, 11 (2015) 515-526.
9. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part II: Dynamic Analysis", *Current Nanoscience*, 11 (2015) 770-783.
10. Marani, R., Perri, A. G., "Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications", *ECS Journal of Solid State Science and Technology*, 5 (2016) M1-M4.
11. Marani, R., Perri, A. G., "A De-Embedding Procedure to Determine the Equivalent Circuit Parameters of RF CNTFETs", *ECS Journal of Solid State Science and Technology*, 5 (2016) M31-M34.
12. Marani, R., Perri, A. G., "A Simulation Study of Analogue and Logic Circuits with CNTFETs", *ECS Journal of Solid State Science and Technology*, 5 (2016) M38-M43.
13. Marani, R., Perri, A. G., "A Comparison of CNTFET Models through the Design of a SRAM Cell", *ECS Journal of Solid State Science and Technology*, 5 (2016) M118-M126.
14. Marani, R., Gelao, G., Perri, A. G., "A Compact Noise Model for C-CNTFETs", *ECS Journal of Solid State Science and Technology*, 6 (2017) M118-126.
15. Marani, R., Perri, A. G., "CNTFET-based Design of Current Mirror in Comparison with MOS Technology", *ECS Journal of Solid State Science and Technology*, 6 (2017) M60-M68.
16. Gelao, G., Marani, R., Perri, A. G., "Effects of Temperature in CNTFET-Based Design of Analog Circuits", *ECS Journal of Solid State Science and Technology*, 7 (2018) M16-M21.
17. Gelao, G., Marani, R., Perri, A. G., "Effects of Temperature in CNTFET-Based Design of Digital Circuits", *ECS Journal of Solid State Science and Technology*, 7 (2018) M41-M48.
18. Gelao, G., Marani, R., Perri, A. G., "Effects of Temperature on Switching Time and Power Dissipation of CNTFET-Based Digital Circuits", *ECS Journal of Solid State Science and Technology*, 7 (2018) M63-M68.
19. Marani, R., Perri, A. G., "Design and Simulation Study of Full Adder Circuit Based on CNTFET and CMOS Technology by ADS", *ECS Journal of Solid State Science and Technology*, 7 (2018) M108-M122.
20. Marani, R., Perri, A. G., "Static Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 121-131.
21. Marani, R., Perri, A. G., "Dynamic Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 277-288.
22. Marani, R., Perri, A. G., "A Review on the Study of Temperature Effects in the Design of A/D Circuits based on CNTFET", *Current Nanoscience*, 15 (2019) 471-480.
23. Marani, R., Perri, A. G., "A Comparison of CNTFET and CMOS technology through the Design of a SRAM Cell", *ECS Journal of Solid State Science and Technology*, 8 (2019) M1-M18.
24. Gelao, G., Marani, R., Perri, A. G., "A Formula to Determine Energy Band Gap in Semiconducting Carbon Nanotubes", *ECS Journal of Solid State Science and Technology*, 8 (2019) M19-M21.
25. Marani, R., Perri, A. G., "A Design Technique of CNTFET-Based Ternary Logic Gates in Verilog-A", *ECS Journal of Solid State Science and Technology*, 8 (2019) M45-M52.
26. Gelao, G., Marani, R., Perri, A. G., "Three-Levels Logic Gates Design Based on CNTFETs", *ECS Journal of Solid State Science and Technology*, 8 (2019) M67-M70.
27. Marani, R., Perri, A. G., "Design of CNTFETs Operating in High Speed Sub-Threshold Condition for Ultra-Low Power Applications", *ECS Journal of Solid State Science and Technology*, 8 (2019) M93-M101.
28. Marani, R., Perri, A. G., "Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits", *ECS Journal of Solid State Science and Technology*, 9 021004 (2020).
29. Marani, R., Perri, A. G., "Techniques to improve the Performance in the CNTFET-based Analogue Circuit Design", *ECS Journal of Solid State Science and Technology*, 9 031001 (2020).
30. Marani, R., Perri, A. G., "Impact of Technology on CNTFET-Based Circuits Performance". ECS Journal of Solid State Science and Technology, 9 051001 (2020).
31. Marani, R., Perri, A. G., "Temperature Dependence of I-V Characteristics in CNTFET Models: A Comparison ", *International Journal of Nanoscience and Nanotechnology*, 17 (2021) 33-39.
32. Marani, R., Perri, A. G., "Comparative analysis of noise in current mirror circuits based on CNTFET and MOS Devices", *International Journal of Nanoscience and Nanotechnology*, 17 (2021) 121-129.

33. Gelao, G., Marani, R., Perri, A. G., “Analysis of Limits of CNTFET Devices through the Design of a Differential Amplifier”, *ECS Journal of Solid State Science and Technology*, 10 061009 (2021).
34. Marani, R., Perri, A. G., “Study of CNTFETs as Memory Devices”, *ECS Journal of Solid State Science and Technology*, 11 031001 (2022).
35. Marani, R., Perri, A. G., “Analysis of Noise in Current Mirror Circuits Based on CNTFET and MOSFET*”, ECS Journal of Solid State Science and Technology*, 11 031006 (2022).
36. Marani, R., Perri, A. G., “Design of a Novel Full Adder Circuit based on CNTFET Technology”, *ECS Journal of Solid State Science and Technology*, 11 051004 (2022).
37. Marani, R., Perri, A. G., “Design and Characterization of Digital Gates based on CNTFET and CMOS Technology*”, ECS Journal of Solid State Science and Technology*, 11 071004 (2022).
38. Gelao, G., Marani, R., Perri, A. G., “Study of Power Gain Capability of CNTFET Power Amplifier in THz Frequency Range*”, ECS Journal of Solid State Science and Technology*, 11 081005 (2022).
39. Marani, R., Perri, A. G., “Noise Effects in the Design of Digital Circuits based on CNTFET*”, ECS Journal of Solid State Science and Technology*, 11 111006 (2022).
40. Marani, R., Perri, A. G., “Noise Effects in the Design of Analog Circuits based on CNTFET*”, ECS Journal of Solid State Science and Technology*, 11 121010 (2022).
41. Gelao, G., Marani, R., Perri, A. G., “Effect of CNT Parameter Variations on CNTFET Amplifier Performance*”, ECS Journal of Solid State Science and Technology*, 12 011004 (2023).
42. Marani, R., Perri, A. G., “A Technique, Based on Thevenin Equivalent Method, to Study the Noise Performance of Analog Circuits Involving both CNTFET and MOS Devices”, *International Journal of Nanoscience and Nanotechnology*, 19 (2023) 9-19.
43. Marani, R., Perri, A. G., “Review—Simulation of A/D Circuits Based on CNTFETs both in SPICE and Verilog-A*”, ECS Journal of Solid State Science and Technology*, 12 031002 (2023).
44. Marani, R., Perri, A. G., “Critical Analysis of CNTFET-Based Electronic Circuits Design*”, ECS Journal of Solid State Science and Technolog*y, 12 051005 (2023).
45. Marani, R., Perri, A. G., “A Review on Static and Dynamic Characterization of Digital Circuits in CNTFET and CMOS Technology”, *International Journal of Nanoscience and Nanotechnology*, 19 (2023) 97-108.
46. http://bsim.berkeley.edu/models/bsim4/, BSIM Group, Berkeley, University of California, USA, (2020).
47. Deng, J., Wong, H.-S. P., “A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region”, *.IEEE Transactions on Electron Devices*, 54 (2007) 3186-3194.
48. Deng, J., Wong, H.-S. P., “A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking”, *IEEE Transactions on Electron Devices*, 54 (2007) 3195-3205.
49. Lee, C-S., Pop, E., Franklin, A.D., Haensch, W., Wong, H.-S. P., “A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nmRegime—Part I: Intrinsic Elements”, *IEEE Transactions on Electron Devices*, 62 (2015) 3061-3069.
50. Lee, C-S., Pop, E., Franklin, A.D., Haensch, W., Wong, H.-S. P., “A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nm Regime—Part II:Extrinsic Elements, Performance Assessment,and Design Optimization”, *IEEE Transactions on Electron Devices*, 62 (2015) 3070-3078.
51. Verilog-AMS language reference manual, Version 2.2, (2014).
52. Raychowdhury, A., Mukhopadhyay, S., Roy, K., “A circuit-compatible model of ballistic carbon nanotube field-effect transistors”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 23 (2004) 1411-1420.
53. Pregaldiny, F., Lallement, C., Kammerer, J. B., “Design-oriented compact models for CNTFETs”, *International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006.*, Tunis, Tunisia, (2006) 34-39.
54. Prégaldiny, F., Lallement, C., Diange, B., Sallese, M., Krummenacher, M., *Compact Modeling of Emerging Technologies with VHDL-AMS*. Huss SA, editor, *Advances in Design and Specification Languages for Embedded Systems*, Dordrecht: Springer Netherlands, ISBN: 978-1-4020-6147-9, (2007).
55. Datta S., *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering 3. Electronic Transport in Mesoscopic Systems*, New York: Cambridge University Press, Online ISBN: 978051180577, (1995).
56. Avouris, P., Chen, Z., Perebeinos, V., “Carbon Based Electronics”, *Nature Nanotechology,* 2 (2007) 605-615.
57. Javey, A. *et al., “*High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates*”, Nature Mater,* 1 (2002) 241-246.
58. Perri, A. G., *“Fondamenti di Elettronica*”, Editor Progedit, Bari, Italy, ISBN:978-88-6194-045-1, (2012).