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A Review on Static and Dynamic Characterization of Digital Circuits in CNTFET and CMOS Technology

Roberto Marani[1] and Anna Gina Perri[2,*]

[1]Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy, 70125, Bari, Italy
[2]Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, 70126, Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
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Abstract

In this paper we review a procedure to characterize digital circuits in CNTFET and CMOS technology in order to compare them. To achieve this goal, we use a semi-empirical compact CNTFET model, already proposed by us, and the BSIM4 model for MOS device. After a brief review of these models, as example, we review the static and dynamic characterization of NAND gate and Full Adder, using the software Advanced Design System (ADS) which is compatible with the Verilog-A programming language. The obtained results allow to highlight the differences between the two technologies.

Keywords: *CNTFET, MOSFET, Modelling, Digital circuits, Verilog-A.*

1. INRODUCTION

We have been dealing with Carbon NanoTubes (CNTs) [1] and Carbon Nano Tube Field Effect Transistors (CNTFETs) [2-11] for many years now. In particular we have studied extensively MOSFET-like CNTFET for high-performance and low-power memory designs [12-21].

In this paper we review a procedure to characterize digital circuits in CNTFET and CMOS technology. As examples we examine a NAND gate and a Full Adder, using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [22].

For CNTFET model, we use a compact, semi-empirical model, already proposed by us [2-3], while, for the MOSFET model, we use the BSIM4 one of ADS library. BSIM (Berkeley Short-channel IGFET Model) [23] refers to a family of MOSFETs for integrated circuit design.

The presentation is organized as follows.

Section 2 gives a brief review of CNTFET and MOSFET models used, while, in Sections 3 and 4, we present the obtained results for the NAND gate in CNTFET and CMOS technology respectively, together with the description of the setup-work used during the simulations.

In Section 5 we review the design and characterization of a Full Adder in both technologies.

Finally Section 6 gives the conclusions and future developments.

2. A BRIEF REVIEW OF CNTFET AND MOSFET MODELS

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them.

The model, based on the hypothesis of ballistic transport, makes reference to [24] and on the following improvements introduced in [25-26] to solve some numerical problems of the original paper [24].

In this Section we just describe the main equations on which our I-V model is based.

The total drain current I_{DS} in our model has been expressed as in [27]:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT}, have the expressions reported in [2-3].

Regarding the C-V model, an exhaustive description of our C-V model is widely described in our References [2-3] and therefore, also in this case, the reader is requested to consult them, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are widely explained:

$$\begin{cases} C_{GD} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behavior, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

We have achieved this goal using an empirical method exhaustively described in [2-3], where we explained that V_{FB}, R_D, R_S have been determined by a best-fit procedure between the measured and simulated values of I-V characteristics of the device, while the quantum capacitances have been computed from the charge in the channel. In this way all elements of the CNTFET equivalent circuit, shown in Figure 1, are determined.

It is similar to a common MOSFET model and is characterized by the generator V_{FB}, for accounting the flat band voltage, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

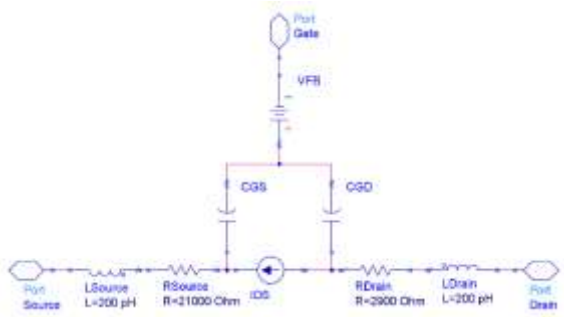

Figure 1. *Equivalent circuit of a n-type CNTFET.*

Other authors [28-29] have then assumed these parameters fixed to constant and typical values (i.e. V_{FB} = 0 V [28] and $R_D = R_S$ = 25 kΩ [29]), thus losing the dependence on the CNT diameter.

Regards to the CNT quantum inductance, as shown in Figure 1, we have assumed constant and equal to 4 pH/nm, which we have splitted up into two inductances of 2 pH/nm, while the classical self-inductance, as it is known [28], can be ignored.

As already said, for the MOSFET model we use the BSIM4 model of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [23] refers to a family of MOSFETs for integrated circuit design. In this work BSIM4 has been used for the 32 nm technology nodes. The MOSFET parameters for BSIM4 model were obtained by Predictive Technology Model (PTM) web site from the Nanoscale Integration and Modelling Group of Arizona State University. In particular we have selected MOSFET sizes in order to obtain output characteristics comparable to those of CNTFET.

3. STATIC AND DYNAMIC ANALYSIS OF LOGIC GATES IN CNTFET TECHNOLOGY

Referring to an inverter, for a static analysis we can determine the voltage transfer characteristic, VTC (Figure 2), and then the noise margins, which provide a measure of the maximum external voltage noise that can be overlapped to the input signals, without causing unwanted output variation [15].

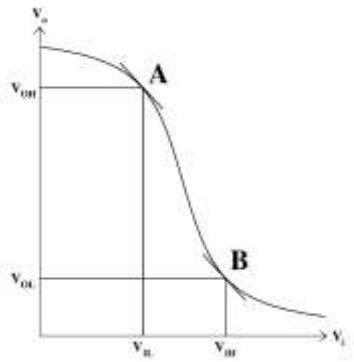

Figure 2. *Voltage transfer characteristic for an inverter.*

The noise margins, whose values are necessary in the design of digital circuits, are determined from the -1 slope points on the VTC, indicated by the letters A and B in Figure 2, which delimit the amplification range of the device. V_{OH} and V_{IL} (point A) represent respectively the valid minimum output voltage at high level and the valid maximum input voltage at low level. Similarly V_{OL} and V_{IH} (point B) the valid maximum output voltage at low level and the valid minimum input voltage at high level.

The noise margins are defined as follows:

$NM_H = V_{OH} - V_{IH}$ for high voltage

and

$NM_L = V_{IL} - V_{OL}$ for low voltage.

When the input voltage V_I is between V_{IL} and V_{IH}, the logic gate is in an undefined state, which is an operative condition that we must avoid to make sure the logic levels are within well-defined regions.

To analyze the dynamic behavior of a logic gate [16], for example an inverter, the parameters of interest are the propagation delay and the rise and fall times (see Figure 3) [30].

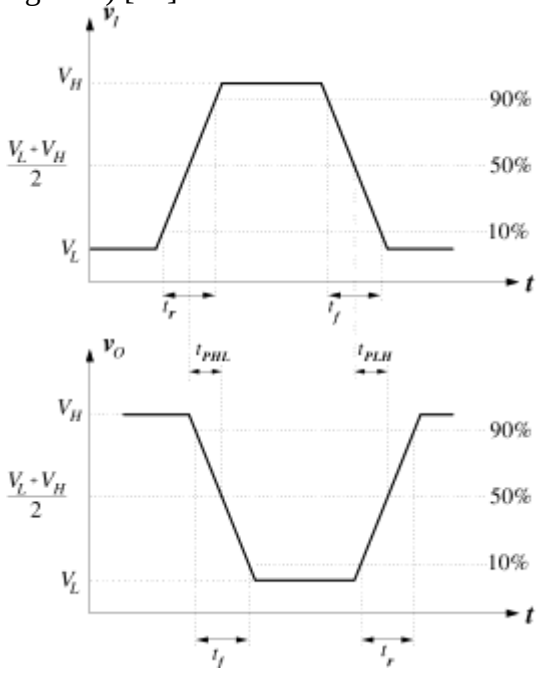

Figure 3. *Time and voltage definitions for input and output waveforms.*

The **rise time t_r** for a given signal is defined as the time required for the signal to make the transition from the 10% point to the 90% point on the waveform, during the V_L-V_H transition. Similarly, **the fall time t_f** is defined as the time required for the signal to make the transition between the 90% point and the 10% point on the waveform, during the V_H-V_L transition.

The 10% and 90% points are defined as follows:

$V_{10\%} = V_L + 0.1\Delta V$

$V_{90\%} = V_L + 0.9\Delta V$

where $\Delta V = V_H - V_L$ is the logic swing, V_H and V_L are the high and low logic levels respectively.

The **propagation delay τ_P** is defined as the difference in time between the input and output signals reaching the 50% points in their respective transitions. The 50% point is the voltage level corresponding to one-half the total transition between V_H and V_L:

$V_{50\%} = (V_H + V_L)/2$

We indicate propagation delay on the high-to-low output transition with τ_{PHL} and that of the low-to-high transition with τ_{PLH}.

As example, we report the schematic of CNTFET NAND gate in Figure 4, while for a NOT gate we advice the reader to see our References [15-16].

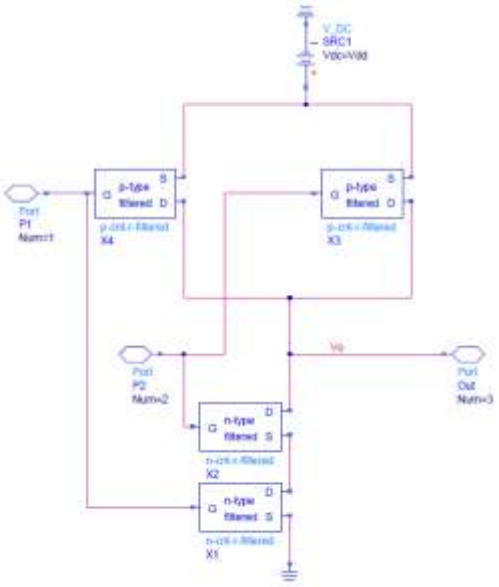

Figure 4*. Schematic of NAND gate in CNTFET technology.*

In this circuit we used a single-supply, denoted as Vdd.

To evaluate the logic port performance, we made a DC simulation [15], changing the voltage supply value and the trans-characteristics are reported in Figure 5, 6, 7, 8 and 9, for different supply voltage values and sweeping Vgs from 0 V to Vdd.

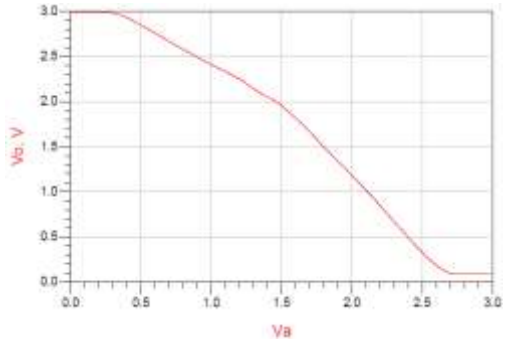

Figure 5*. Trans-characteristic at Vdd = 3 V.*

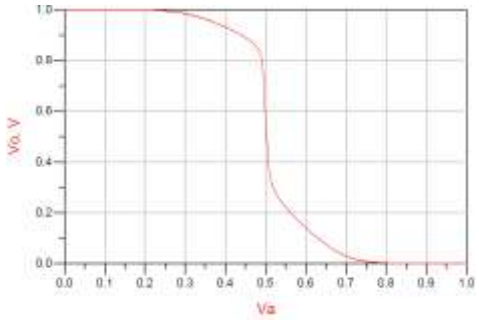

Figure 6*. Trans-characteristic at Vdd = 1 V.*

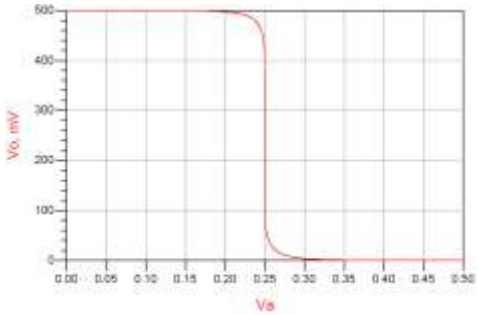

Figure 7*. Trans-characteristic at Vdd = 0.5 V.*

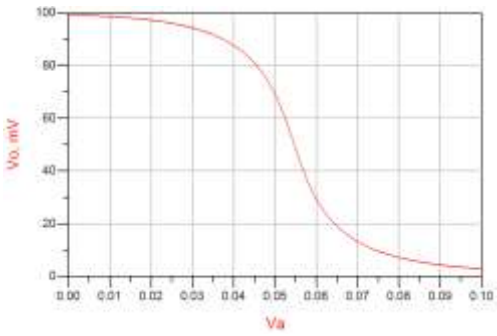

Figure 8*. Trans-characteristic at Vdd = 0.1 V.*

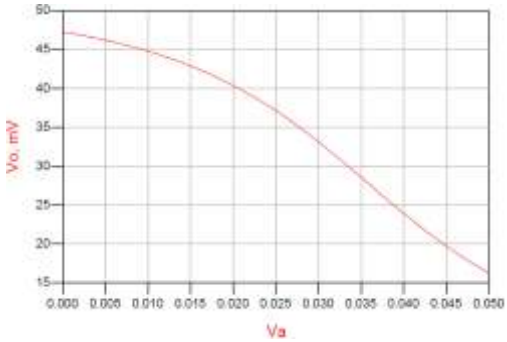

***Figure 9**. Trans-characteristic at Vdd = 0.05 V.*

For supply voltage smaller than 0.1V, the rigenerate characteristic is worse than 0.5 V and greater supply voltage, as shown in the previous Figures. Moreover, for 0.05 V supply voltage the logic port presents a trans-characteristic that does not allow the correct mode of operation because there is not a clear division between the high logic state and the low logic state.

Figure 10 allows to evaluate the propagation delay of the NAND gate [16].

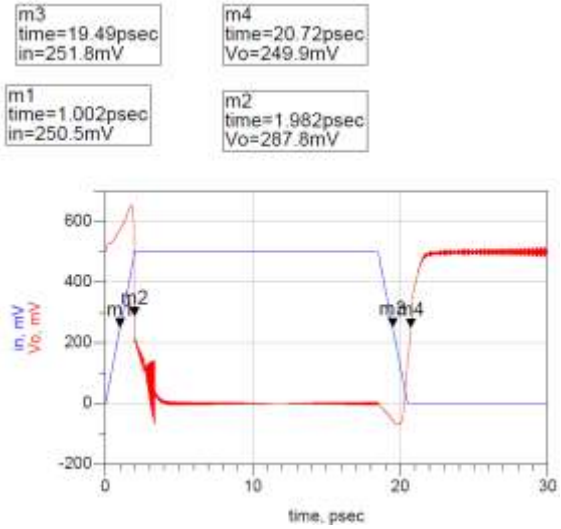

***Figure 10**. Propagation Time Evaluation.*

According to the previous definitions, the propagation delay τ_P, for the reviewed example is equal to about 1.12 ps.

4. STATIC AND DYNAMIC ANALYSIS OF LOGIC GATES IN CMOS TECHNOLOGY

Figure 11 shows the schematic of NAND gate in CMOS technology.

Also in this circuit we used a single-supply (Vdd). To evaluate the logic port performance, we made a DC simulation, changing the voltage supply value, and sweeping Vgs from 0 V to Vdd.

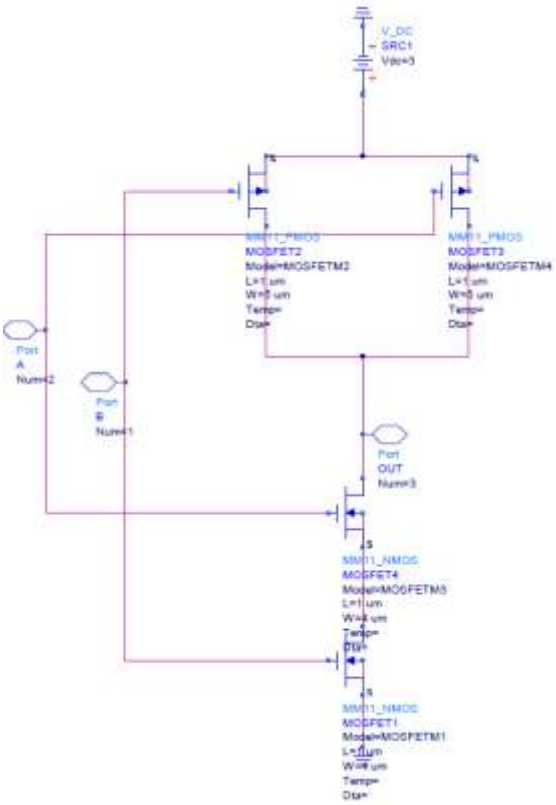

***Figure 11**. Schematic of NAND gate in CMOS technology.*

In order not to burden the discussion, we limit ourselves to reporting the obtained trans-characteristics at Vdd = 3 V. as shown in Figure 12.

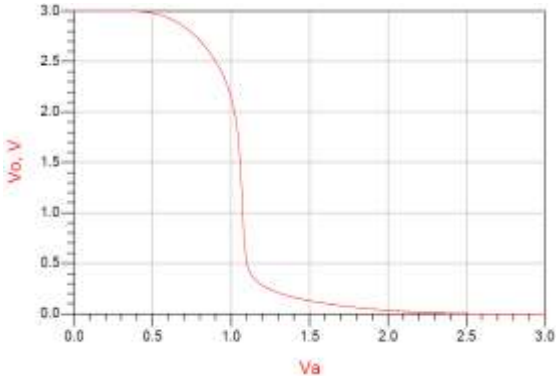

***Figure 12**. Trans-characteristic at Vdd = 3 V.*

Similarly, Figure 13 allows to evaluate the propagation delay of the NAND gate in CMOS technology.

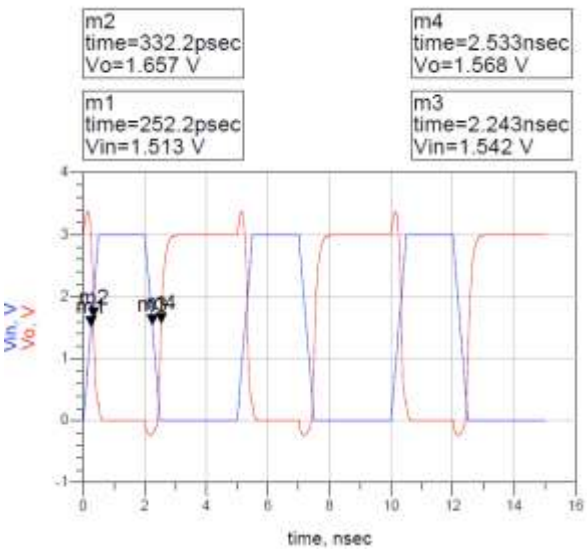

***Figure 13**. Propagation Time Evaluation.*

According to the previous definitions, the propagation delay τ_P in this case is equal to about 180 ps.

It is possible observe that the CNTFET devices are quicker than CMOS having less time delay and greater work frequency then CMOS.

Moreover the lower voltage supply for CNTFET allows the development of low power applications.

5. FULL ADDER CIRCUIT DESIGN AND CHARACTERIZATION

A Full Adder [30] adds binary numbers and has three inputs and two outputs. The two inputs are A and B, and the third input is a carry input C_{IN}. The output carry is designated as C_{OUT}, and the normal output is designated as S_{UM}.

The truth table of the full adder circuit is shown in Figure 14.

A	B	C_{IN}	C_{OUT}	S_{UM}
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

***Figure 14**. Truth table of a Full Adder.*

The circuit of Figure 15 realizes the function proposed by truth table.

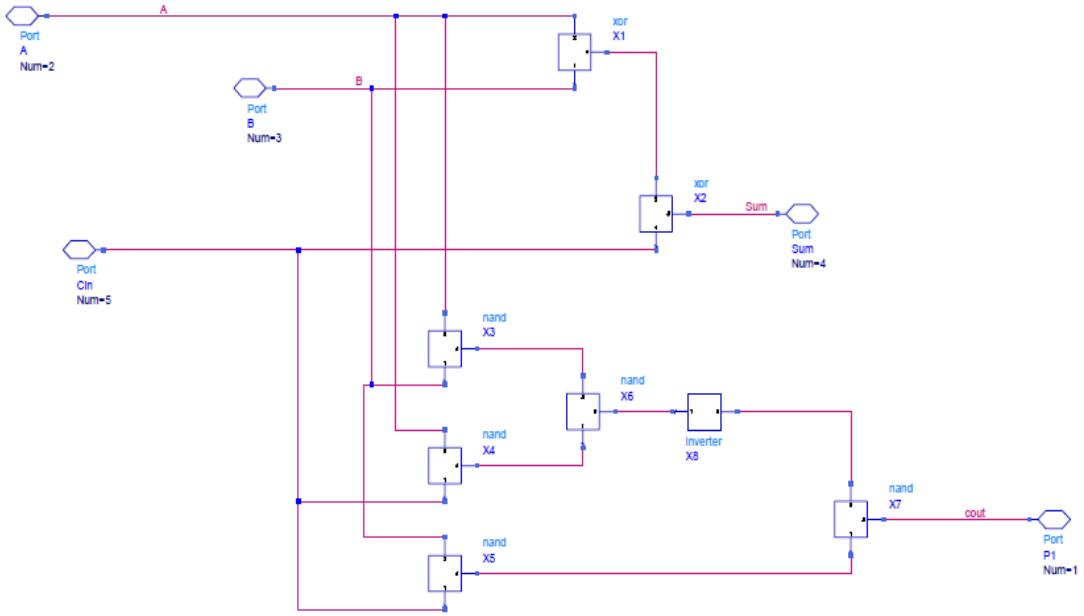

***Figure 15**. Full adder schematic.*

where XOR gate is realized with NAND gates, as the schematic of Figure 16.

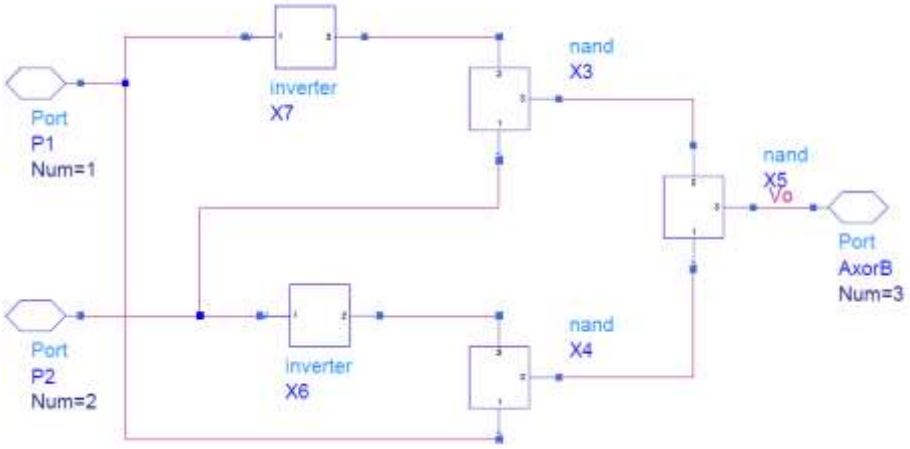

Figure 16*. XOR schematic.*

5.1 Full adder design in CNTFET technology

The simulations to verify the correct mode of operation of full adder, have been made, doing compromise choice.

As we have widely illustrated in [15-16], for a supply voltage of 0.5 V the NAND and NOT gates present a VTC that allows the correct mode of operation because there is a clear division between the high logic state and the low logic state. Therefore in our simulations we have fixed a supply voltage of 0.5 V.

Assuming Cin = 1 for all simulations, in Figures 17, 18, 19 and 20 we show output and input signals of the full adder at 1 GHz, 30 GHz, 50 GHz and 80 GHz, respectively

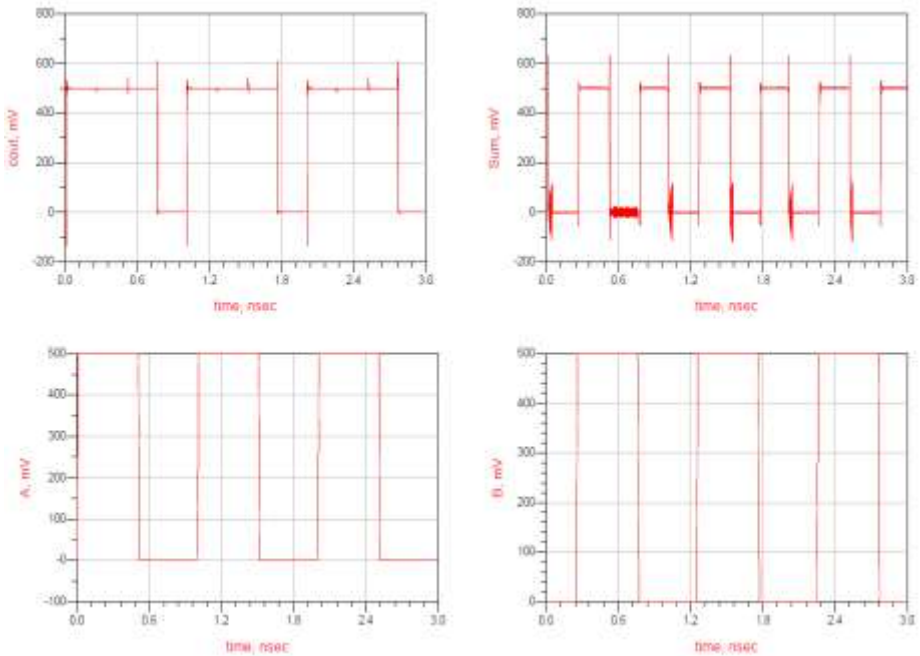

Figure 17*. Output and input signals of the full adder at 1 GHz.*

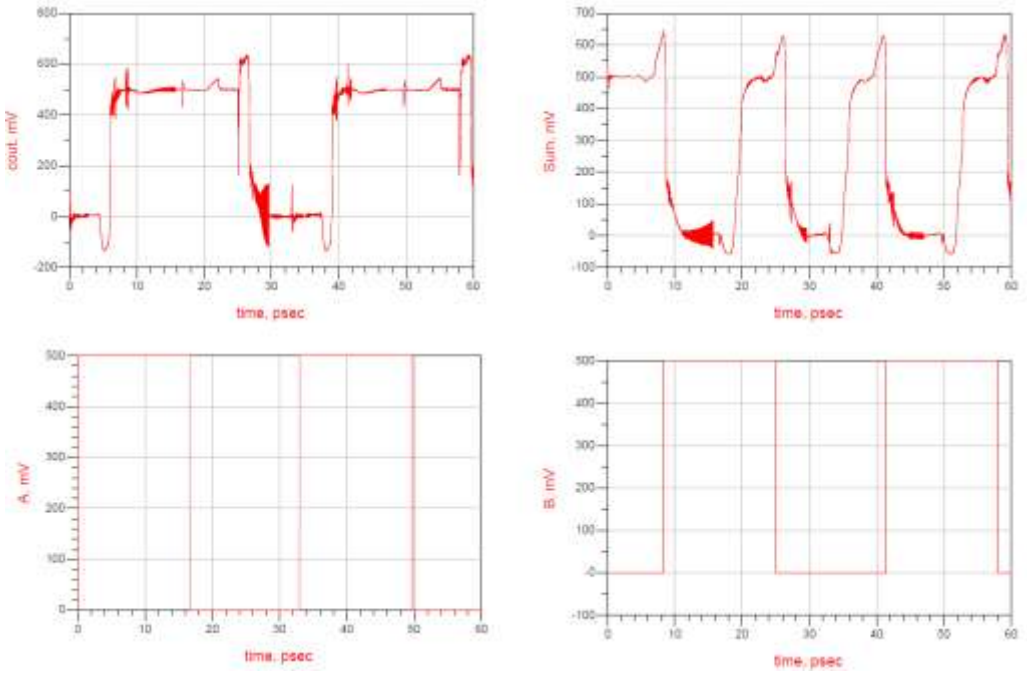

***Figure 18**. Output and input signals at 30 GHz.*

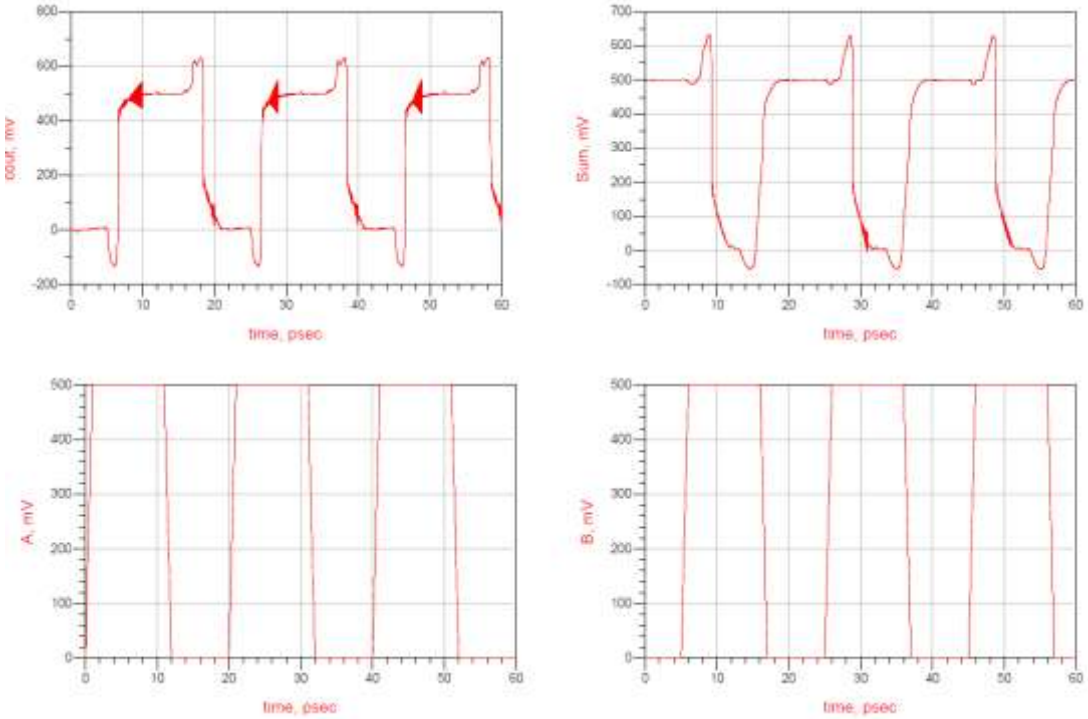

***Figure 19**. Output and input signals at 50 GHz.*

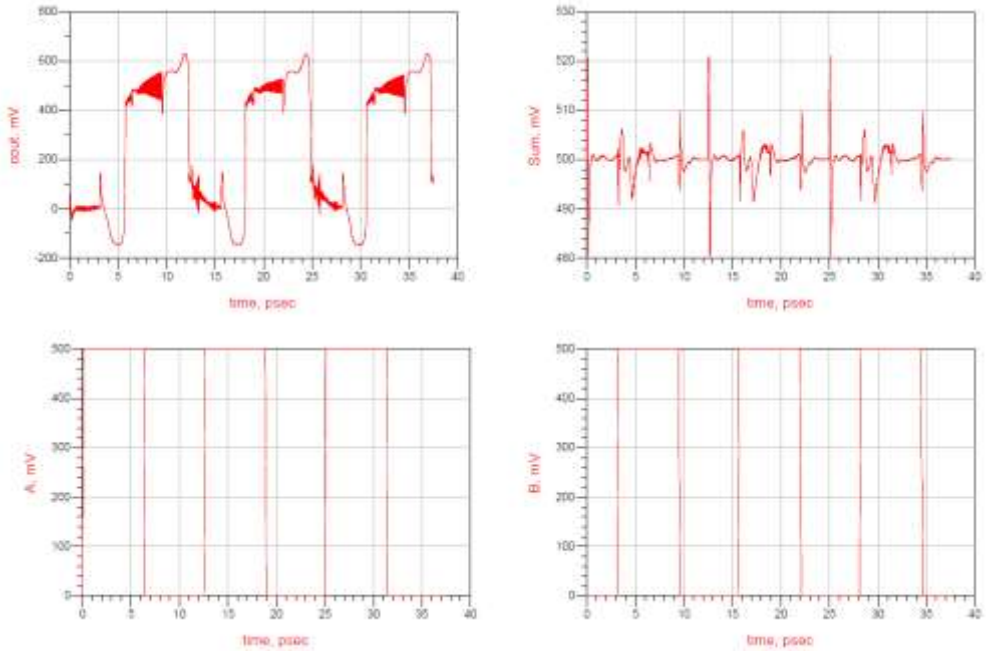

***Figure 20**. Output and input signals at 80 GHz.*

From the analysis of the previous figures, we can affirm that the limit for a correct mode of operation is 50 GHz. In fact, with a frequency of 80 GHz (Figure 20), the output S_{UM} completely loses its meaning.

5.2 Full Adder Design in CMOS Technology

In this case, as we have widely illustrated in [15-16], for a supply voltage of 3 V the NAND and NOT gates present a VTC that allows the correct mode of operation because there is a better frequency characteristic. Therefore in our simulations we have fixed a supply voltage of 3 V.

For Cin = 1 for all simulations, in Figures 21, 22 and 23 we show output and input signals of the full adder at 100 MHz, 200 MHz and 333 MHz, respectively.

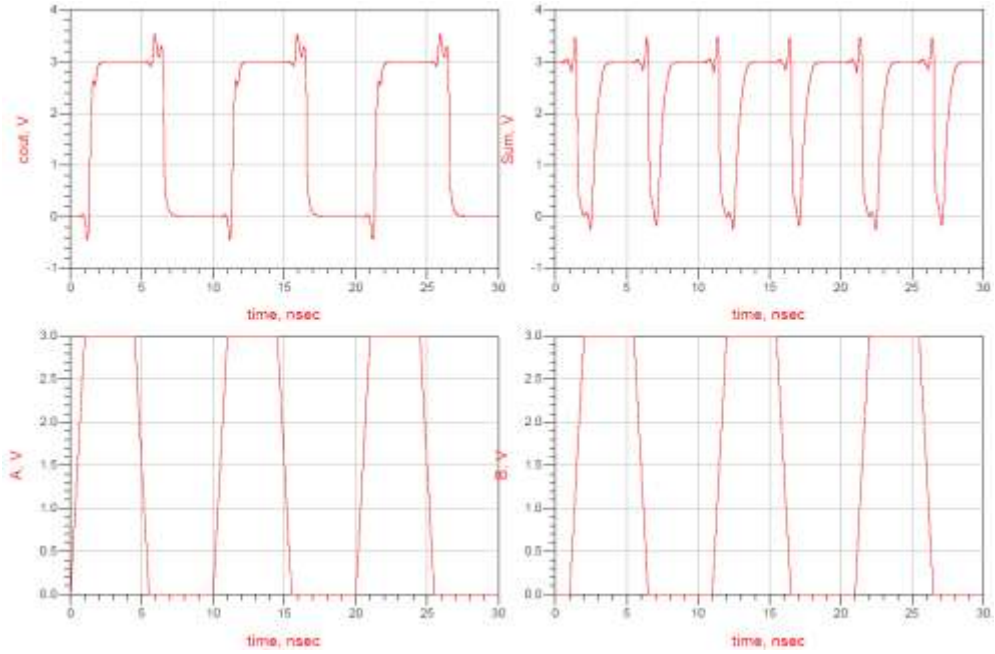

***Figure 21**. Output and input signals at 100 MHz.*

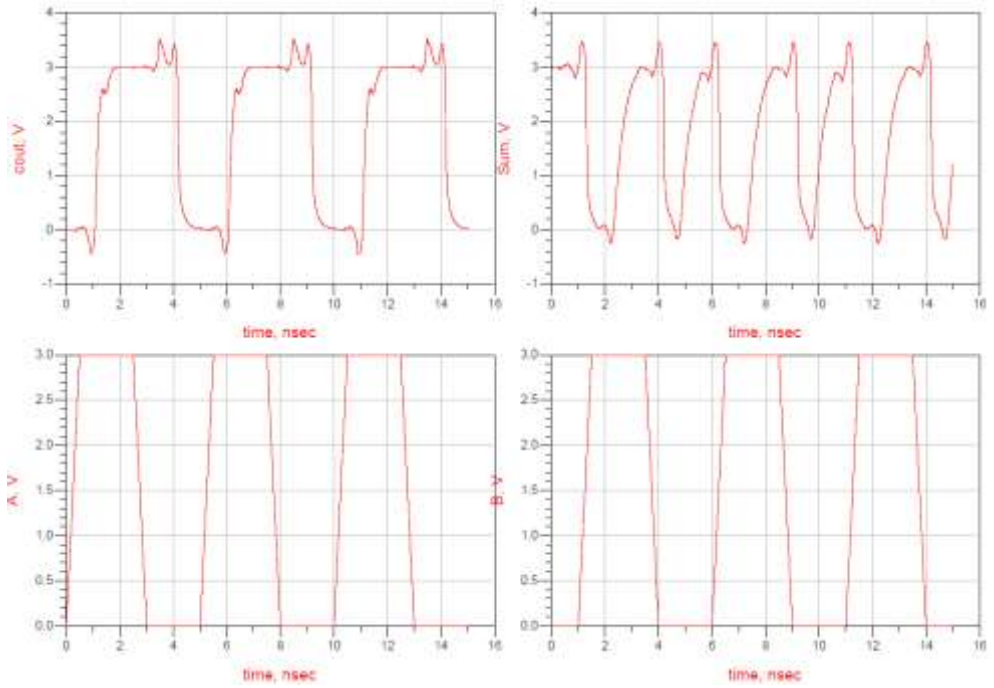

***Figure 22**. Output and input signals at 200 MHz.*

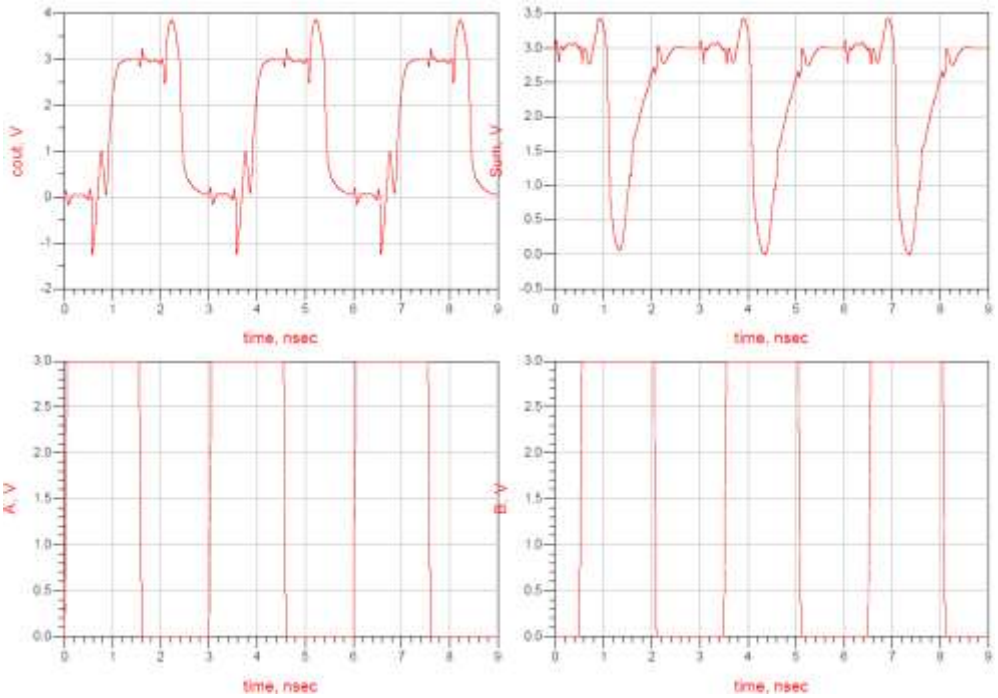

***Figure 23**. Output and input signals at 333 MHz.*

For CMOS technology the limit for a correct mode of operation is 200 MHz. In fact with a frequency of 333 MHz, (Figure 23), the output S_{UM} completely loses its meaning.

Definitely the optimal results have been at 0.5 V and 50 GHz for CNTFET, while for CMOS technology at 3 V and 200 MHz.

6. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we reviewed a procedure to characterize digital circuits in CNTFET and CMOS technology in order to compare them. To achieve this goal, we used a semi-empirical compact CNTFET model, already proposed by us, and the BSIM4 model for MOS device. As example we reviewed the static and dynamic characterization of a NAND gate and a Full Adder in both technologies, using the software Advanced Design System (ADS). The obtained results allowed to highlight the differences between the two technologies.

Moreover we want to emphasize that the reviewed procedure can be applied to analyze any other digital circuit.

Currently we are working to study the CNTFETs as memory devices [31] and as power amplifier [32], continuing to explore the effects of temperature [33-34] and of noise [35-37] in other circuits based on CNTFETs. Moreover we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [38] and the impact of technology on CNTFET-based circuits performance [39-40].

We also intend to repeat the proposed simulations using other CNTFET models such the model proposed in literature [41-42] in order to have comparable results.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. Marani, R., Perri, A. G., "CNTFET Modelling for Electronic Circuit Design", *Electro Chemical Transactions*, 23 (2009) 429 - 437.
2. Gelao, G., Marani, R., Diana, R., Perri, A. G., "A Semi-Empirical SPICE Model for n-type Conventional CNTFETs", *IEEE Transactions on Nanotechnology*, 10 (2011) 506-512.
3. Marani, R., Perri, A. G., "A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software", *Current Nanoscience*, 7 (2011) 245-253.
4. Marani, R., Perri, A. G., "A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications", *International Journal of Electronics*, 99 (2012) 427 - 444.
5. Marani, R., Gelao, G., Perri, A. G., "Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design", *Microelectronics Journal*, 44 (2013) 33-39.
6. Marani, R., Perri, A. G., "Modelling of CNTFETs for Computer Aided Design of A/D Electronic Circuits", *Current Nanoscience*, 10 (2014) 326-333.
7. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis", *Current Nanoscience*, 11 (2015) 515-526.
8. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part II: Dynamic Analysis", *Current Nanoscience*, 11 (2015) 770-783.
9. Marani, R., Perri, A. G., "Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications", *ECS Journal of Solid State Science and Technology*, 5 (2016) M1-M4.
10. Marani, R., Perri, A. G., "A De-Embedding Procedure to Determine the Equivalent Circuit Parameters of RF CNTFETs", *ECS Journal of Solid State Science and Technology*, 5 (2016) M31-M34.
11. Marani, R., Perri, A. G., "A Simulation Study of Analogue and Logic Circuits with CNTFETs", *ECS Journal of Solid State Science and Technology*, 5 (2016) M38-M43.
12. Marani, R., Perri, A .G., "A Comparison of CNTFET Models through the Design of a SRAM Cell", *ECS Journal of Solid State Science and Technology*, 5 (2016) M118-M126.
13. Marani, R., Perri, A. G., "CNTFET-Based Design of Current Mirror in Comparison with MOS Technology", *ECS Journal of Solid State Science and Technology*, 6 (2017) M60-M68.
14. Marani, R., Perri, A. G., "Design and Simulation Study of Full Adder Circuit Based on CNTFET and CMOS Technology by ADS", *ECS Journal of Solid State Science and Technology*, 7 (2018) M108-M122.
15. Marani, R., Perri, A. G., "Static Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 121-131.
16. Marani, R., Perri, A. G., "Dynamic Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 277-288.
17. Gelao, G., Marani, R., Perri, A. G., "Effects of Temperature in CNTFET-Based Design of Analog Circuits", *ECS Journal of Solid State Science and Technology*, 7 (2018) M16-M21.

18. Gelao, G., Marani, R., Perri, A. G., "Effects of Temperature in CNTFET-Based Design of Digital Circuits", *ECS Journal of Solid State Science and Technology*, 7 (2018) M41-M48.
19. Marani, R., Perri, A. G., "A Review on the Study of Temperature Effects in the Design of A/D Circuits based on CNTFET", *Current Nanoscience*, 15 (2019), 471-480.
20. Marani, R., Perri, A. G., "Temperature Dependence of I-V Characteristics in CNTFET Models: A Comparison", *International Journal of Nanoscience and Nanotechnology*, 17 (2021) 33-39.
21. Gelao, G., Marani, R., Perri, A. G., "Effect of CNT Parameter Variations on CNTFET Amplifier Performance", *ECS Journal of Solid State Science and Technology*, 12 (2023) 011004.
22. Verilog-AMS language reference manual, Version 2.2, (2014).
23. http://bsim.berkeley.edu/models/bsim4/, BSIM Group, Berkeley, University of California, USA, (2020).
24. Raychowdhury, A., Mukhopadhyay, S., Roy, K., "A circuit-compatible model of ballistic carbon nanotube field-effect transistors", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 23 (2004) 1411-1420.
25. Pregaldiny, F., Lallement, C., Kammerer, J. B., "Design-oriented compact models for CNTFETs", *International Conference on Design and Test of Integrated Systems in Nanoscale Technology, DTIS 2006*, Tunis, Tunisia, (2006) 34-39.
26. Prégaldiny, F., Lallement, C., Diange, B., Sallese, M., Krummenacher, M., *Compact Modeling of Emerging Technologies with VHDL-AMS*. Huss SA, editor, *Advances in Design and Specification Languages for Embedded Systems*, Dordrecht: Springer Netherlands, ISBN: 978-1-4020-6147-9, (2007).
27. Datta S., *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering 3. Electronic Transport in Mesoscopic Systems*, New York: Cambridge University Press, Online ISBN: 978051180577, (1995).
28. Avouris, P., Chen, Z., Perebeinos, V., "Carbon Based Electronics", *Nature Nanotechology*, 2 (2007) 605–615.
29. Javey, A. *et al., "*High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates*", Nature Mater*, 1 (2002) 241–246.
30. Perri, A. G., *Fondamenti di Elettronica*, Editor Progedit, Bari, Italy, ISBN:978-88-6194-045-1, (2012).
31. Marani, R., Perri, A. G., "Study of CNTFETs as Memory Devices", *ECS Journal of Solid State Science and Technology*, 11 (2022) 031001.
32. Gelao, G., Marani, R., Perri, A. G., "Study of Power Gain Capability of CNTFET Power Amplifier in THz Frequency Range", *ECS Journal of Solid State Science and Technology*, 11 (2022) 081005.
33. Marani, R., Perri, A. G., "Review—Thermal Effects in the Design of CNTFET-Based Digital Circuits", *ECS Journal of Solid State Science and Technology*, 11 (2022) 041006.
34. Gelao, G., Marani, R., Perri, A. G., "A Formula to Determine Energy Band Gap in Semiconducting Carbon Nanotubes", *ECS Journal of Solid State Science and Technology*, 8 (2019) M19-M21.
35. Marani, R., Perri, A. G., "Noise effects in the Design of Digital Circuits Based on CNTFET", *ECS Journal of Solid State Science and Technology*, 11 (2022) 031006.
36. Marani, R., Perri, A. G., "Noise Effects in the Design of Analog Circuits Based on CNTFET", *ECS Journal of Solid State Science and Technology*, 11 (2022) 121010.
37. Marani, R., Perri, A. G., "A Technique, Based on Thevenin Equivalent Method, to Study the Noise Performance of Analog Circuits Involving both CNTFET and MOS Devices", *International Journal of Nanoscience and Nanotechnology*, 19 (2023) 9-19.
38. Marani, R., Perri, A. G., "Editors' Choice—Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits", *ECS Journal of Solid State Science and Technology*, 9 (2020) 021004.
39. Marani, R., Perri, A. G., "Impact of Technology on CNTFET-Based Circuits Performance", *ECS Journal of Solid State Science and Technology*, 9 (2020) 051001.
40. Gelao, G., Marani, R., Perri, A. G., "Analysis of Limits of CNTFET Devices through the Design of a Differential Amplifier", *ECS Journal of Solid State Science and Technology*, 10 (2021) 061009.
41. Lee, C-S., Pop, E., Franklin, A.D., Haensch, W., Wong, H.-S. P., "A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nmRegime—Part I: Intrinsic Elements", *IEEE Transactions on Electron Devices*, 62 (2015) 3061-3069.
42. Lee, C-S., Pop, E., Franklin, A.D., Haensch, W., Wong, H.-S. P., "A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nm Regime—Part II:Extrinsic Elements, Performance Assessment,and Design Optimization", *IEEE Transactions on Electron Devices*, 62 (2015) 3070-3078.