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Low Power and Low Latency Phase-Frequency Detector in Quantum-Dot Cellular Automata Nanotechnology

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Abstract

Nowadays, one of the most important blocks in telecommunication circuits is the frequency synthesizer and the frequency multipliers. Phase-frequency detectors are the inseparable parts of these circuits. In this paper, it has been attempted to design two new structures for phase-frequency detectors in QCA nanotechnology. The proposed structures have the capability of detecting the phase differences of the rising edge or falling edge of their inputs. Also, it can detects frequency differences of its two inputs. In the design of proposed PFDs D flip-flop with few number of cells, area and low delay is used. The proposed PFD circuits in QCA technology have 159 quantum cells, 0.2 μm2 of occupied area, and 1 clock cycle delay for reset path. In comparison to the previous PFD in QCA technology, the proposed designs have ability to detect phase differences more than half of the period of reference signal. That means the capture range of them are approximately 4π (between -2π to 2π). Also, the power simulation of the proposed structures of phase-frequency detector is presented in this paper.

Keywords: *PFD, QCA, Power, Delay, Phase-Frequency detector.*

1. INRODUCTION

Nowadays, with the advances in electronics, along with the limitations of the electronic devices, there seems to be a crucial need for new technologies that can overcome these limitations [1]. Limitations such as maximum operating frequency, power consumption, data transfer rate, and occupied area in technologies such as CMOS technology have become increasingly problematic. One of the new technologies that is expected to be able to overcome these limitations is the emergent quantum-dot cellular automata (QCA) nanotechnology [2]. Recent researches indicate that this technology is able to operate desirably at frequencies much higher than previous technologies such as CMOS, with a smaller occupied area and faster speed [3]. Many designs are done for digital circuits in QCA technology, such as full adder, multiplexer, decoder [4, 5] and flip flops.

One of the important elements of any communication system is the frequency synthesizer section [6]. Frequency synthesizers have several types, with delay-locked loop (DLL) and phase-locked loop (PLL) being the most common ones [7, 8]. One of the inseparable elements in DLL and PLL structures is the phase-frequency detector (PFD) [9, 10]. The phase-frequency detector circuit is actually responsible for determining, and ultimately, modifying the phase difference between the input and output signals of frequency synthesizer. Also, PFD can determine the frequency differences of two signals. Since this block is an inseparable part of a frequency synthesizer, it is considered as the basis of the design in this paper. Phase-frequency detectors have

many limitations that can eventually lead to undesirable behaviors in the frequency synthesizer and therefore, in the entire transmitter and receiver system. Examples of these limitations include the maximum operating frequency limitation, the smallest measurable phase difference, static phase error, power consumption, and dead-zone [11, 12]. It seems that these problems can be overcome to some extent with the aid of the new QCA technology. Therefore, the aim of this paper is to design a new phase-frequency detector in QCA technology with desirable performance characteristics.

Since D flip-flops with reset pins are used in the phase-frequency detector structure, and due to the fact that the phase-frequency detector circuit has not been designed in QCA technology to date, it is worthy to investigate the articles that have focused on D flip-flops with reset pins. In [13], two D flip-flops with reset capability are proposed that suffer from high cell number and large occupied area. These structures also are equipped with reset capability outside the main flip-flop structure. Also, a structure for flip-flop with reset ability is proposed in [14], which has two major drawbacks, namely high cell number and its problem for using in larger circuits such as a phase-frequency detector. In [15] and [16], flip flops with reset ability are proposed, whose circuit area have increased slightly due to the presence of reset pin, and the number of the occupied cells can still be reduced. Therefore, this paper, a D flip-flop with reset capability, proposed by the authors of this paper in their previous design [17], is used which functions suitably with respect to previous works in terms of cell number, delay, and occupied area. Therefore, the primary aim of this paper is to design a new phase-frequency detector in QCA technology based on D lip-flop with reset technology that can provide optimum conditions in terms of delay, power consumption and number of consumed quantum cells. Only one work is done in this domain [18]. In [18] a new PFD is designed in QCA technology. Although the proposed design in [18] has some good features but it has one main drawback which limit its application. The designed PFD of [18] just can detect the phase differences smaller than half of the period of reference signal since they choose the topology with this limitation. That means the capture range of it is about 2π (between $-\pi$ to $+\pi$) In the proposed PFDs of this paper the PFDs have ability to detect phase differences more than half of the period of the reference signal and the capture range of the work is approximately 4π (between -2π to $+2\pi$).

This paper is organized as follows: in the next section, the main concepts of QCA are presented. Afterwards, in the third section, the proposed phase-frequency detector structure is introduced. The fourth section is concerned with simulations and results; and finally, the fifth section concludes this paper.

2. BASIC CONCEPTS IN QCA

In the emergent QCA technology, similar to any other new technology, new concepts are presented. In this technology, each quantum cell consists of 4 quantum dots and 2 electrons that can move between these 4 quantum dots (Fig.1). Also, as electrons move according to Coulomb's law, two stable states can be considered for quantum cells, recognized as logic zero and logic one (Fig.1). The wiring in the QCA is also achieved readily by placing quantum cells in series [19]. The NOT gate and the majority gate could be mentioned as the basic gates in this technology [19]. The AND and OR gates are also derivatives of the majority gate [20]. It is worth noting that information transmission in QCA technology occurs under four distinct clock phases, which actually control the data transmission path [20].

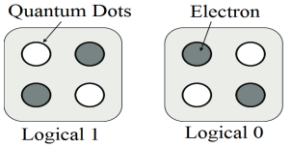


Figure 1. *Basic QCA cells.*

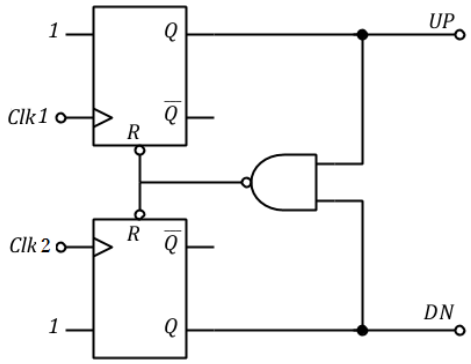


Figure 2. *Block diagram of conventional PFD.*

3. THE STRUCTURE OF THE PROPOSED PHASE-FREQUENCY DETECTOR

The phase-frequency detector is one of the most important blocks in communication circuits such as PLL and DLL. The block diagram of a common phase-frequency detector is shown in Fig.2. As can be observed, a phase-frequency detector is generally comprised of two D-type flip-flops, whose outputs are applied to flip-flops' reset through AND gate (if reset of flip-flop is activated by logic one) or NAND gate (if the reset of flip-flop in activated by logic zero). The function of a phase-frequency detector in determining the phase difference of rising edges is such that if, for example, the rising edge of signal A first comes first, the output of the corresponding flip-flop becomes logic one and remains in this state. When the rising edge of signal B comes up, both flip-flop outputs become logic one for a moment and the flip-flop reset will be activated and both outputs will become zero. In this case, the output UP and its pulse width will indicate the extent to which signal A is ahead of B. Therefore, the greater the phase difference, the wider the pulses created at the outputs. If B is ahead of A, the pulse width of DN output will be created proportional to a phase difference of two inputs signals. The aim of this paper is to design a phase-frequency detector in QCA technology.

The proposed structure of phase-frequency detector for determination of the phase difference of the rising edges in QCA technology is shown in Fig.3. Considering the length of the reset path of the proposed structure, it is evident that in the feedback path, both the outputs UP and DN of Fig.2 remain in logic one state with the same delay as the reset path. Therefore, to properly observe the phase difference of the two signals at the outputs UP and DN, it is necessary to rectify this matter. To this end, a circuit is used at the output of the structure to rectify the PFD operation. The block diagram of proposed PFD to cover these issues is shown in Fig.3.

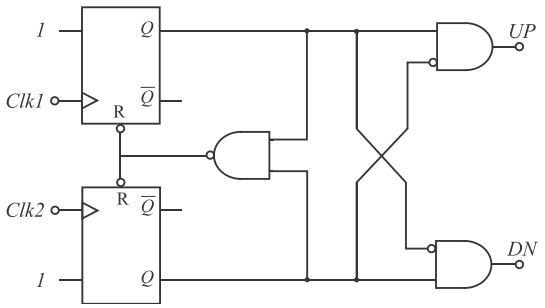
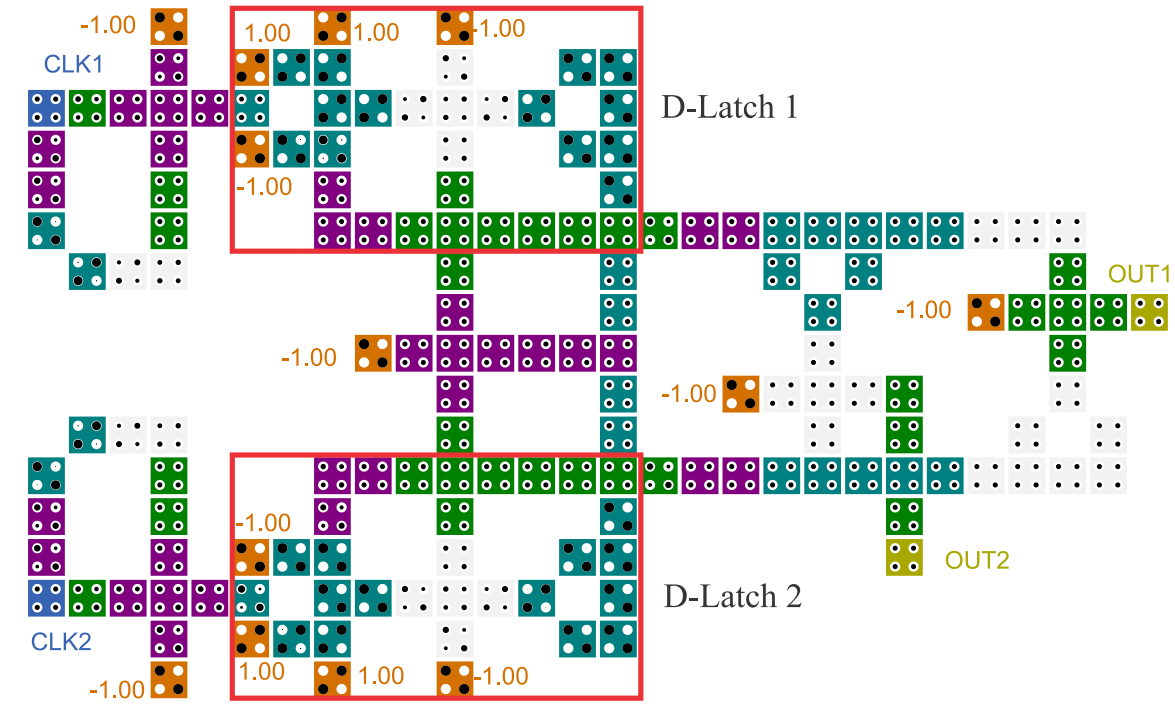


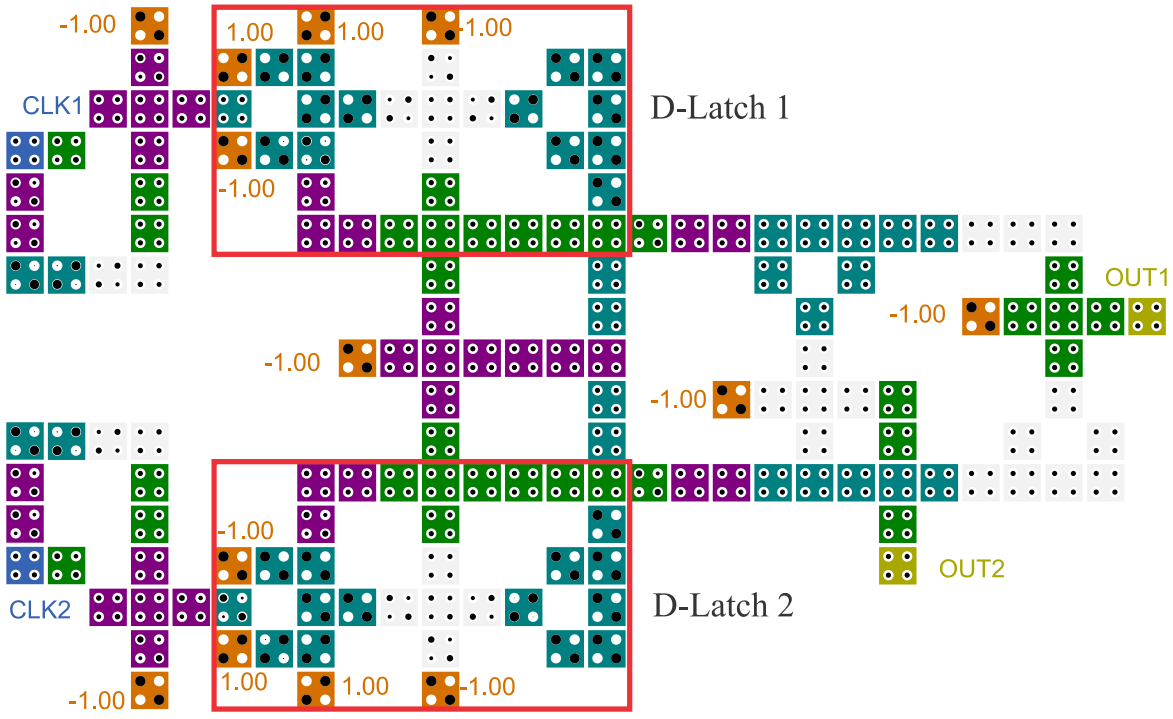
Figure 3. *Block diagram of proposed PFD to be design in QCA technology.*

These issues and the different parts of phase-frequency detector circuit for determination of the phase difference of the rising edges in QCA technology are specified in Fig.4.a. It should be mentioned that the D-latch structure is also shown in this figure. In the design of flip flop circuit, a 2:1 multiplexer is used.

By creating feedback from the multiplexer output to its input, a memory loop is created so that if the select multiplexer input is zero, it keeps the output constant. By applying the select input of the multiplexer to logical one, the other input of multiplexer acts as an input of D-latch and the value of it will be sent directly to the output and stored in the memory loop [17].



(a)



(b)

Figure 4. *a) Proposed PFD in QCA nanotechnology to detect rising edge phase differences, b) Proposed PFD in QCA nanotechnology to detect falling edge phase differences.*

In addition to have reset feature to the structure of D-latch an AND gate with one inversed input is used in the memory loop [17]. It should be noted that the reset of proposed design is active high. Level to edge converter is used to convert D-latch

to D flip-flop (edge sensitive). All of these can be seen in Fig.4.a. The proposed structure consists of 159 quantum cells and has a reset path delay of 1 QCA clock cycle, and the input to output delay is equal to 2.25 QCA clock cycles. The proposed structure of PFD in QCA technology for determination of the phase difference of the falling edges is shown in in Fig.4.b. It should be mentioned that the D-latch structure is also shown in this figure. The behavior of this circuit is similar to the previous structure, except that the difference between falling edges among the two inputs is measured by the circuit.

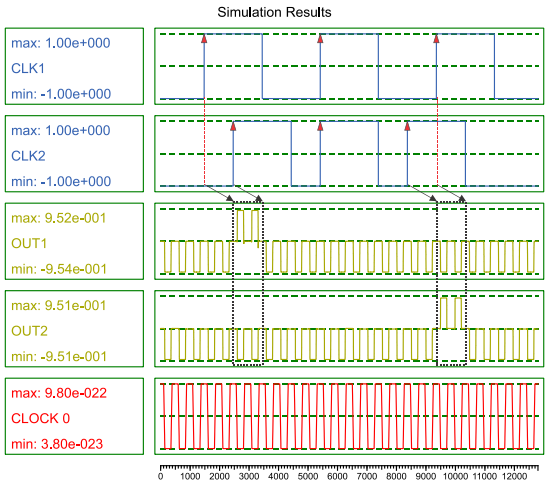


Figure 5. *Simulation results of proposed PFD in QCA nanotechnology for detecting phase differences of rising edges in three different cases.*

4. SIMULATION AND RESULTS

The proposed structures in QCA technology is simulated by QCADesigner and QCAPro software to verify circuit performance and power dissipation, respectively. Fig.5 shows the simulation results of the proposed PFD structure in QCA technology to determine the phase difference of the rising edges in three different states: CLK1 being ahead of CLK2, two input signals being in-phase, and CLK1 lagging behind CLK2. As can be observed, when signal CLK1 is ahead of CLK2 at the rising edges by two QCA clock cycles, only the signal at the output UP appears at exactly two QCA clock cycles. Moreover, in the second part of this figure, when the rising edges of the two signals are simultaneous, there is no logic one pulse width in either of the two outputs. Finally, according to the figure, when signal CLK1 is lagging by two clock cycles behind signal CLK2, a pulse width of two QCA clock cycles appears at the DN output and the UP output is zero. In other words, according to this simulation, the pulse width at UP indicates how advanced signal CLK1 is with respect to CLK2 and the pulse width at DN indicates how lagged signal CLK1 is with respect to CLK2. Additionally, when the signals are in-phase, there is no pulse width at UP or DN.

Also, Fig.6 shows the simulation results of the proposed PFD structure in QCA technology for determination of the frequency difference of the rising edges when the CLK1 and CLK2 signals have dissimilar frequencies. In this case, UP or DN outputs are activated depending on which rising edge occurs earlier. As can be observed in Fig.5, CLK1 is initially ahead of CLK2 by two clock cycles of the input, and the corresponding output is generated at UP. Then, at the second and third rising edge of the two signals, CLK2 advances from CLK1 to CLK1 by 4 and 10 QCA clock cycles, respectively, and therefore, a proportional phase difference appears as pulse width at the DN output. This demonstrates the appropriate function of the proposed circuit at different frequencies of the two inputs.

Fig.7 also shows the case in which the PFD input signals have a phase difference of more than half a period. The appropriate function of the circuit is again confirmed in this case by the output forms. The importance of this issue lies in the fact that the XOR gate can itself be used as a phase detector, but its weakness is its inability to detect phase differences of over 180 degrees.

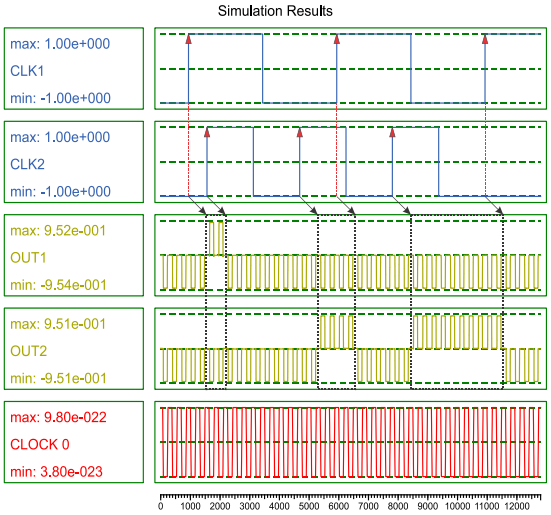


Figure 6. *Simulation results of proposed PFD in QCA nanotechnology for detecting frequency differences of rising edges in case that inputs frequencies are different.*

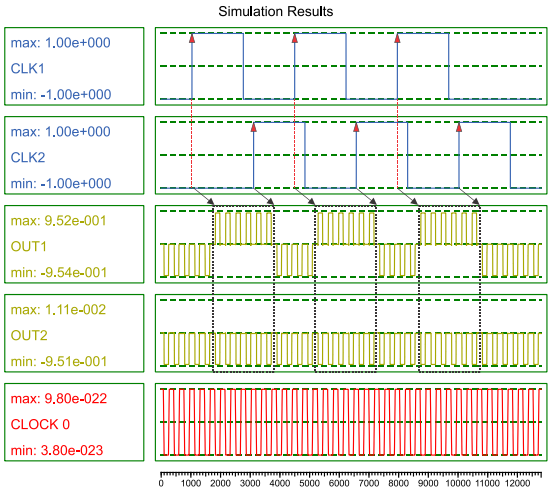


Figure 7. *Detecting the phase differences in case that the phase differences are more than half of period of input signals.*

Fig.8 shows the simulation results of the proposed PFD structure in QCA technology for determination of the phase difference of the falling edges in three different cases: CLK1 being ahead of CLK2, the two input signals being in-phase, and CLK1 lagging behind CLK2 . As can be observed, when the signal CLK1 is ahead of CLK2 at the falling edges by two QCA clock cycles, only the signal at the UP output appears at exactly two QCA clock cycles.

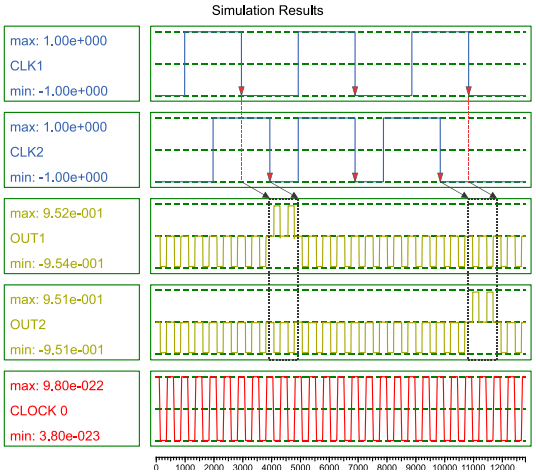


Figure 8. *Simulation results of proposed PFD in QCA nanotechnology for detecting phase differences of falling edges in three different cases.*

Also, in the second part of this figure, when the falling edges of the two signals are simultaneous, there is no logic one in either of the two pulse width outputs. Finally, according to the figure, when the signal CLK1 is lagging behind CLK2 by two QCA clock cycles, a pulse width of two QCA clock cycles emerges at the DN output and the UP output is zero. This wave form confirms the appropriate function of the proposed structure. Other forms obtained by the falling edge-triggered PFD are approximately similar to the falling edge-triggered PFD. Therefore, the results of these simulations are not presented in order to avoid repetition.

Fig.9 and Fig.10 show the results of power dissipation analysis of the proposed structures. Simulations are performed by QCAPro software. In calculating the power dissipation, the same input patterns as in the simulations are used. In these figures, which depict an approximately similar power pattern, points with stronger colors represent greater capacity for power dissipation. Moreover, Table-1 shows the switching and dissipation energies of the proposed circuits for different values of E_K.

5. CONCLUSIONS

In this paper, two new structures for phase-frequency detectors were presented. One of these detectors is capable of detecting the phase difference between the rising edges of the two input signals, and the other is capable of detecting the phase difference between the falling edges. The proposed structures have 159 quantum cells, 0.2 um^2 of occupied cross area, and 1 reset delay cycle. The design principles of quantum cells have been considered in designing the desired structures. It is worth mentioning that the phase-frequency detector structures are designed for the first time in QCA technology, which can be used as the basis of more complex circuit designs.

Table 1. *Average leakage and switching energy dissipation of proposed designs for different E_K.*

	Average Leakage Energy dissipation			Average Switching Energy Dissipation		
	$0.50E_K$	$1.00E_K$	$1.50E_K$	$0.50E_K$	$1.00E_K$	$1.50E_K$
Proposed rising edge sensitive PFD	0.05370	0.15532	0.27264	0.03771	0.03068	0.02511
Proposed falling edge	0.05337	0.15523	0.27289	0.03748	0.02999	0.02413

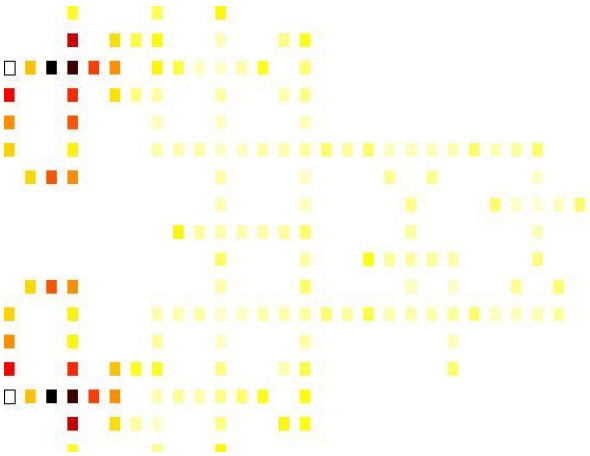


Figure 9. *Energy dissipation diagram of proposed PFD sensitive to rising edges.*

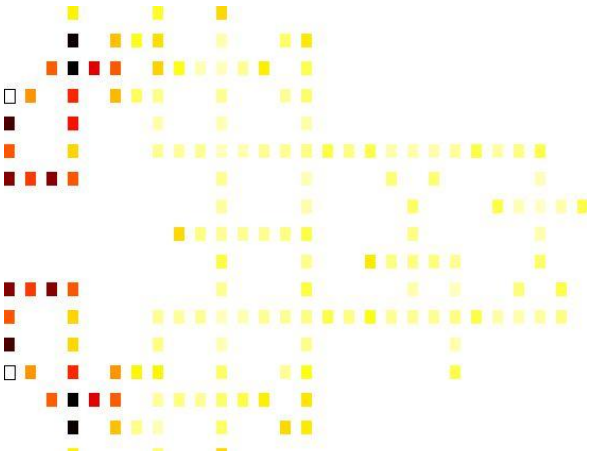


Figure 10. *Energy dissipation diagram of proposed PFD sensitive to falling edges.*

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