Improved Thermal Stability of NiSi Nanolayer in Ni-Si Co-sputtered Structure

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Abstract:

Electrical, structural and morphological properties of Ni silicide films formed in Ni(Pt 4at.%)/Si(100) and $Ni_{0.6}Si_{0.4}$(Pt 4at.%)/Si(100) structures at various annealing temperatures ranging from 200 to 1000 °C were studied. The Ni(Pt) and $Ni_{0.6}Si_{0.4}$(Pt) films with thickness of 15 and 25 nm were deposited by RF magnetron co-sputtering method, respectively. The annealing process of the structures was performed by using a long time annealing (LTA) procedure for 30 min. The samples were analyzed by four point probe sheet resistance (R_s) measurement, x-ray diffraction (XRD) and atomic force microscopy (AFM) techniques. It was found that the thermal stability as well as the surface morphology of "as-formed" Ni silicide nanolayers depends on annealing temperature. Ni silicide nanolayers formed in the $Ni_{0.6}Si_{0.4}$(Pt)/Si systems are more thermally stable as compared to those formed in the Ni(Pt)/Si systems during LTA procedure. It was also determined that the NiSi phase with R_s value of about 4 Ω/□ is formed in a wide temperature range from 400 to 900 °C. Indeed, the addition of Si during the Ni deposition restricts the agglomeration of NiSi layer and retards phase formation of $NiSi_2$. According to AFM morphological analysis, NiSi layers formed in the $Ni_{0.6}Si_{0.4}$(Pt)/Si systems at high temperatures have low average surface roughness and can be used as a contact material in nanometric scale.
Keywords: *Nickel monosilicide (NiSi), Thermal stability, Surface roughness, Sputtering, Contact layer*

1. INTRODUCTION

During recent years, the rapid development of microelectronic technology has been realized through minimization and integration of the electronic devices. But with reduction of device dimensions, the contact resistance of interfaces increases, thus, the proper material selection with a low resistivity is essential for the future devices. The choice of metal silicides in Si technology is straightforward, because they meet the basic requirements including low specific resistivity, low contact resistance to both n and p-types of Si, high thermal stability, and good process compatibility with the standard Si technology [1].

Among the various silicides, $TiSi_2$ has been the most studied material due to its wide usage for complementary metal-oxide semiconductor (CMOS) metallization. For line widths lower than 0.5µm, $TiSi_2$ was replaced by $CoSi_2$. This replacement is due to the fact that the formation of the low-resistivity phase of $TiSi_2$ depends on the line width. Instead, $CoSi_2$ can grow epitaxially on a Si substrate, using a post annealing process [2,3,4]. For sub-100nm technology, $TiSi_2$ and $CoSi_2$ are expected to be replaced by Nickel monosilicide. NiSi has some advantages over $TiSi_2$ and $CoSi_2$ such as line width independence, low electrical

resistivity (13.6μΩ-cm) and a relatively low Si consumption. Therefore, NiSi can be considered as an attractive candidate material for use in modern CMOS fabrication process as nanometric contacts [1-5].

The main disadvantage of NiSi is its poor thermal stability which limits its application. Formation of NiSi and its transition to the high resisted $NiSi_2$ phase [6] occurs at around 350 and 750°C, respectively. Thus, it is necessary to improve thermal stability of NiSi significantly by adding small amount of other alloying metals like Pt [7,8,9], Co [10], Ir [11], Ta [12], Ti [13, 14], and P [15] to the deposited Ni layer. This improvement can be also achieved by using an interlayer between the Ni layer and the Si substrate [16,17] or capping layer [18]. In addition to the phase transition from NiSi to $NiSi_2$, agglomeration of the NiSi thin film with increasing temperature and decreasing film thickness also limits the application of NiSi as nanometric contacts [19]. Thus, NiSi thin films with excellent thermal stability at high temperatures are essential for future device applications.

In this work, we have investigated the thermal stability and some physical properties including electrical properties, surface roughness and phase formation of NiSi layers produced in the both Ni(Pt 4at.%)/Si(100) and $Ni_{0.6}Si_{0.4}$(Pt 4at.%)/Si(100) structures at different temperatures in a long time annealing procedure.

2. EXPERIMENTAL

The experiments were carried out on p-type Si(100) wafers as substrates with resistivity of 8-10Ω-cm and size of 10×10mm^2. After a standard RCA substrate cleaning procedure, it followed by a 60s dip in a diluted HF solution ($HF:H_2O$=1:20 in volume), the substrates were dried and loaded into a vacuum chamber. The sputtering chamber was evacuated to a base pressure less than 1×10^{-6} Torr prior to the sputtering process. We have used RF magnetron co-sputtering technique with a Ni target of 50mm in diameter to fabricate desired silicides. The geometrical details of the experimental set up can be found elsewhere [20].

In order to deposit the $Ni_{0.6}Si_{0.4}$ (Pt 4at. %) structure, three pieces of Si and Pt with area of 10×10 and 5×1 mm^2 were symmetrically placed on the Ni target, respectively. The discharge power of the deposition process was maintained at about 50 W that resulted in a deposition rate of about 10nm/min. During the deposition, a dynamic flow of an ultrahigh purity Ar gas with a pressure of 10 mTorr was used for the sputtering discharge. The thickness of the deposited $Ni_{0.6}Si_{0.4}$ (Pt 4at. %) was considered about 25nm which was monitored in-situ by a quartz crystal oscillator and measured by an optical technique. To make a comparison, 15 nm Ni(Pt 4at.%) thin films with a similar procedure were deposited on the Si(100) substrate. By considering thickness of 15 and 25nm for the Ni(Pt) and $Ni_{0.6}Si_{0.4}$(Pt) structures, respectively, the amount of Ni in both deposited layers was kept identical. The proportion of the elements in the deposited layers was determined by X-ray photoelectron spectroscopy (XPS).

The post annealing process of the samples was performed in an N_2 ambient with a flow rate of 0.5 lit/min in a temperature range from 200 to 1000°C. The temperature was measured by a Pt-Rh thermocouple connected to a Al_2O_3 boat adjacent to the samples. In this work, the samples were heated in long time annealing (LTA) treatment. In this process, the sample was heated with a rate of 0.5^{o}C/s from the room temperature until it reaches the desired temperature. Then, the desired temperature was maintained for 30 min. Finally, the furnace was turn off and the system cooled down to the room temperature.

Four Point Probe sheet resistance (R_s) measurements were utilized to investigate the electrical properties of the samples. X-ray diffraction (XRD) with a Cu-Kα radiation source was employed to determine the phase formation and crystallographic orientation of the films as well as the average size of the nanocrystal grains. Surface chemical composition of the samples was characterized by X-ray photoelectron spectroscopy (XPS). The surface morphology and the average roughness of the annealed samples were studied by atomic force microscopy (AFM) with a Si tip having 10 nm in radius in contact mode. All AFM images are obtained in scale of 5×5μm^2 with 256×256 pixel resolution.

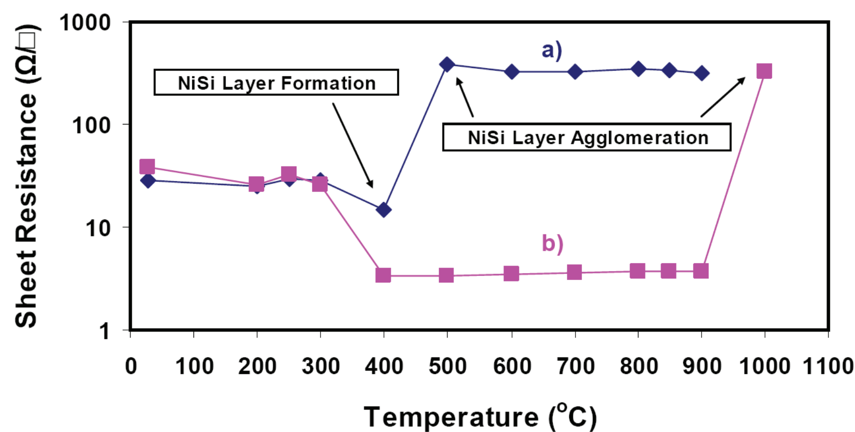

Figure 1: *Logarithmic scale of sheet resistance variation with annealing temperatures for different structures: (a) Ni(Pt 4at.%)/Si(100) and (b)* $Ni_{0.6}Si_{0.4}$*(Pt 4at.%)/Si(100).*

3. RESULTS AND DISCUSSION

3.1. Sheet resistance measurements

Figure 1 shows the behavior of the thermal stability of both systems annealed under the LTA procedure. The R_s value of the Ni(Pt)/Si structure reached to the value of ~14 Ω/□ when it was annealed at 400 °C due to phase formation of NiSi layer at this temperature. Under our experimental conditions for this sample, Ni_xPt_ySi could be formed (x and y > 1), with a high resistance of 22 Ω/□ as reported by others [21]. The formation of the NiSi phase was recently reported under the RTA process at a lower temperature of 400°C [22]. A drastic increase in the sheet resistance of the sample was found after annealing at 500°C which is attributed to agglomeration of the NiSi film [23] in favor of transition to a phase with high resistivity [5]. This agglomeration was also observed in our AFM images at the higher annealing temperatures (see section 3.3).

The sheet resistance of the annealed $Ni_{0.6}Si_{0.4}$(Pt)/Si structure reveals a rather different feature. At first, by increasing the annealing temperature to 200°C, the R_s value slightly decreased, probably due to the condensation of $Ni_{0.6}Si_{0.4}$(Pt) film and the existence of some impurities in it, as similarly observed by others [24]. The rise of the R_s value at 250°C is due to formation of Ni_2Si phase (see also Figure 3). A sudden reduction in the R_s value was found by annealing the $Ni_{0.6}Si_{0.4}$(Pt)/Si structure at 400°C. This reduction is a signature of the phase formation for the NiSi layer at this temperatures [5,6]. Surprisingly, the R_s value remains at the same low level (~4 Ω/□) for the $Ni_{0.6}Si_{0.4}$(Pt)/Si structure up to 900°C. Such behavior indicates substantial formation of a thermally stable NiSi phase. It should be noted that annealing at 1000°C destroys this favorable thermally stable layer which can be observed from the increasing surface roughness (see section 3.3). Therefore, long time annealing of the $Ni_{0.6}Si_{0.4}$(Pt)/Si structure provides formation of a uniform NiSi layer with low R_s value and an excellent thermal stability.

By comparing the data in Figure 1 with our results reported in Ref. [25] where we have used a short annealing process, the most distinct observation is the shift in the NiSi formation temperature. The temperature profile in the short annealing procedure is such that the samples reached at the desired temperatures with high heating rate (20°C/s) leads to formation of a discontinuous layer, especially at high temperatures (900°C) [6]. But in the LTA process, the rate at which the samples reached to the desired temperature is rather small (0.5°C/s) in which there is enough interaction time for interdiffusion of the Ni and Si atoms in the $Ni_{0.6}Si_{0.4}$(Pt)/Si system. The inter-diffusion occurred before agglomeration of the NiSi layer at the high temperatures (> 800°C) and resulted in an improvement of thermal stability

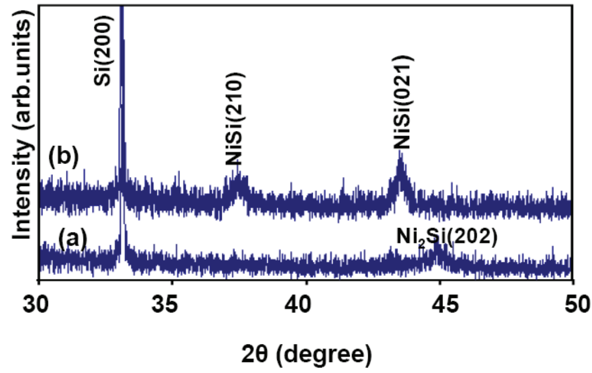

Figure 2: *XRD spectra of the Ni(Pt 4at.%)/Si(100) structure annealed at different temperatures: a) 250 and b) 500 °C.*

for the NiSi layer formed by the LTA process as compared to the layer formed under the short annealing process.

3.2. X-ray diffraction

X-ray diffraction (XRD) was employed to determine the phase formation and crystallographic orientations in the samples annealed at different temperatures. Figure 2 shows XRD patterns of the Ni(Pt)/Si(100) structure annealed by LTA procedure at 250 and 500°C. For the samples annealed at 250°C, there was only one peak with a weak intensity due to formation of a Ni_2Si phase which has a higher resistivity than the nickel monosilicide phase [19]. At 500°C, the reaction between the deposited Ni layer and the Si substrate completed and a NiSi phase with different crystallographic orientations was formed. A similar XRD pattern for the sample annealed at 400°C is also observed under the LTA procedure. Despite the formation of the NiSi phase at 500°C, the sheet resistance of this sample was not low (see Figure 1) which is attributed to severe agglomeration of the NiSi layer, and consequently, formation of discontinuous NiSi grains on the surface.

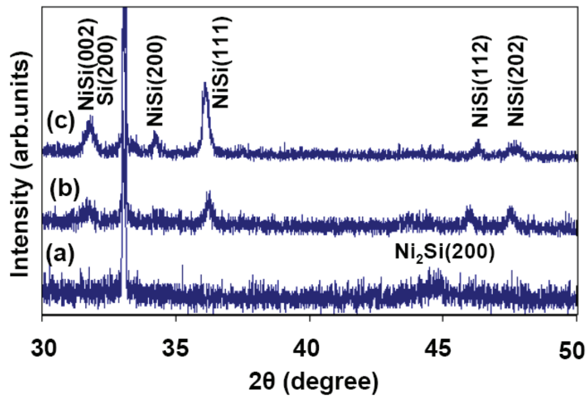

Figure 3: *XRD spectra of the $Ni_{0.6}Si_{0.4}$(Pt 4at.%)/Si(100) structure annealed at different temperatures: a) 250, b) 500 and c) 800 °C.*

Figure 3 shows XRD patterns of the $Ni_{0.6}Si_{0.4}$(Pt)/Si(100) samples annealed at 250, 500 and 800°C. A Ni_2Si phase formed after annealing at 250°C while annealing at higher temperatures such as 500 and 800°C resulted in higher peak intensity of the NiSi indicating formation of substantial amount of the NiSi phase in the layer (Figure 3b and 3c) at these temperatures. It should be noted that for the samples annealed at much higher temperature (800°C), neither the phase transition from NiSi to $NiSi_2$ nor new orientations of the NiSi phase were observed. Since the R_s value of the formed $Ni_{0.6}Si_{0.4}$(Pt) layers are low at higher temperatures as shown in Figure 1, it can be concluded that the film mainly consists of NiSi crystals with different orientations. Minimization of Gibbs free energy is behind the selection of different orientations. We note the difficulties to quantify this process as the required data especially surface energies and their temperature/stress/strain dependence and the presence of impurities are unavailable [26,27].

Based on the XRD analysis, the average size of NiSi crystal grains can be estimated from the all related peaks by utilizing the Scherrer relation stating $d = \frac{0.9\lambda}{\beta\cos(\theta)}$, where λ is the wavelength of the incident radiation (0.154 nm), β is FWHM of the peak in radians after subtracting the instrumental broadening (~0.1°) and θ is the Bragg angle. For determining FWHM of the peaks, after a background subtraction, a single peak was fitted to the peaks based on discussion in Ref [28]. It should be noted that the Scherrer equation gives the size of coherently diffracting domains, rather than the actual grain size. For the Ni(Pt)/Si structure annealed at 500 and 800°C, the size of NiSi crystal

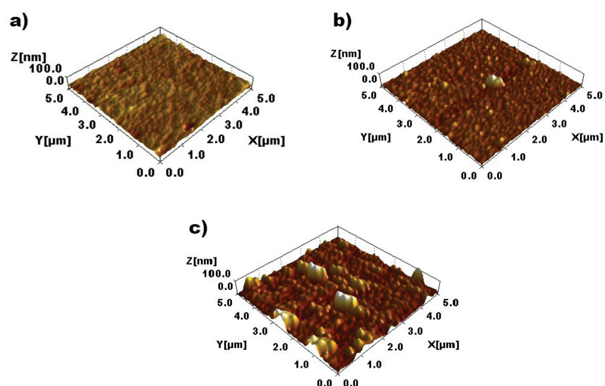

Figure 4: *AFM images of the Ni(Pt 4at.%)/Si(100) surface annealed at different temperatures: a) 400, b) 500, and c) 900 °C.*

grains was determined at about 17±4 and 22±4 nm, respectively. While for the $Ni_{0.6}Si_{0.4}$(Pt)/Si structure under the same annealing conditions, the average size of crystal grains for this system annealed at 500 and 800°C was determined at about 33±4 and 42±7 nm, respectively. Therefore, the crystal grains formed in the annealed $Ni_{0.6}Si_{0.4}$(Pt)/Si structure were larger than the crystal grains in the annealed Ni(Pt)/Si structure prepared under similar conditions.

3.3. AFM analysis

The effect of temperature on the morphology and surface roughness of the annealed samples were studied using AFM technique. Figures 4 demonstrates the contact mode AFM images of the Ni(Pt)/Si(100) structures annealed at different temperatures, respectively. AFM image of the Ni(Pt)/Si(100) sample annealed at 400°C (Fig 4a) shows a smooth surface with abot 5 nm root mean square (RMS) roughness and without any grain boundary formation. As can be observed in Figure 4b, by increasing the annealing temperature to 500°C, grain boundaries formed on the surface with average size of 50 ±25 nm and the surface roughness slightly increased to 6 nm. These are related to the

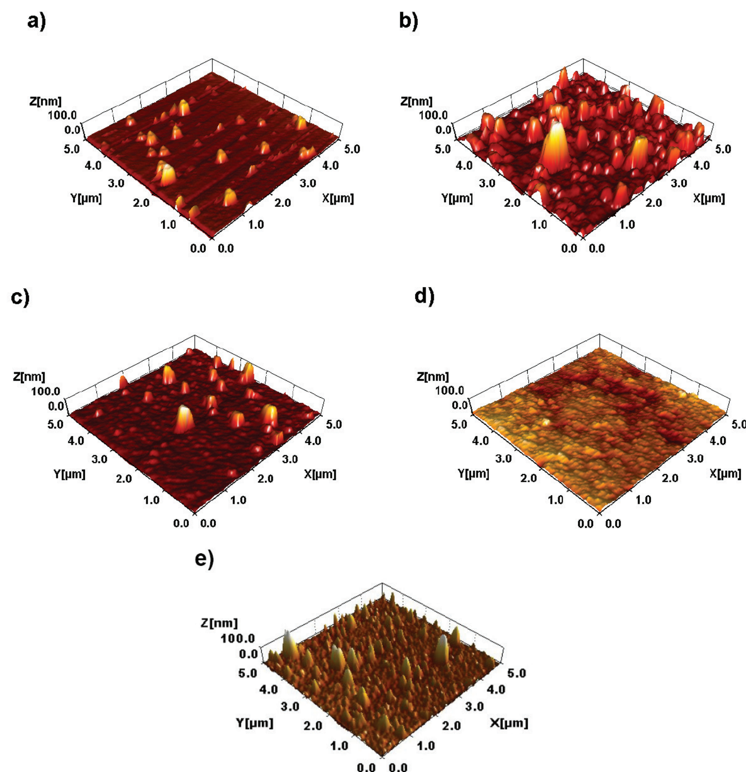

Figure 5: *AFM images of the $Ni_{0.6}Si_{0.4}$(Pt 4at.%)/Si(100) surface annealed at different temperatures: a) 400, b) 600, c) 800, d) 900, and e) 1000 °C.*

agglomeration of the thin film, which were also responsible for the increasing in the sheet resistance measurements (see section 3.1). By increasing the annealing temperature up to 900°C, although the average grain size did not change significantly (60±35 nm), but the surface roughness increased to about 20 nm which can be related to the diffusion of the thin film into the substrate.

From the AFM image analysis for the $Ni_{0.6}Si_{0.4}$(Pt)/Si(100) sample annealed at 400°C (Figure 5a), the surface roughness was determined at about 4 nm. By increasing the annealing temperature to 600°C (Figure 5b), the surface roughness increased to 20 nm. Annealing the samples at the higher temperatures of 800 and 900°C resulted in a reduction of the surface roughness to 8 and 4 nm, respectively. However, after annealing the sample at 1000°C (Figure 5e), the surface roughness increased to 13 nm and its sheet resistance increased dramatically to about 320 Ω/□. A remarkable difference is observed between the surface roughness and the sheet resistance. While surface roughness of the $Ni_{0.6}Si_{0.4}$(Pt)/Si(100) structure annealed at intermediate temperatures, i.e 500 and 600°C, is high, the sheet resistance remains almost unchanged. This can be attributed to diffusion of Ni atoms from the $Ni_{0.6}Si_{0.4}$(Pt) layer into the Si substrate and/or accumulation of the un-reacted deposited Si on the surface. At the higher temperatures, i.e 800 and 900°C, the Si atoms in the film also diffuses resulting in the formation of a more uniform layer.

For the lower annealing temperatures (from 200 to 400°C), the average grain size was determined around 43±10 nm, while a severe increase occurred for the samples annealed at 500°C resulting in formation of grains with average size of 200±100 nm. By further increasing the annealing temperature to 900°C, the size of grains reduced slightly to 170±70 nm which can be related to diffusion of Si atoms from the substrate toward the film surface. As mentioned before, the R_s value of the samples annealed at 900°C is low even after the long annealing time. As observed by Biswas et al. [29], co-sputtering of Si with Ni in proper ratio prevents diffusion of Ni atoms into the substrate, therefore, a low sheet resistance at a higher temperature (up to 900°C) is accessible. Thus, we believe that the co-sputtered Si atoms can bond more easily in an order structure with Ni atoms than Si atoms from the substrate. In absence of co-sputtered Si, for formation of NiSi layer, it needs many Ni atoms to diffuse into the substrate. Hence, the NiSi/Si interface becomes very rough. Therefore, according to our results, we propose that the $Ni_{0.6}Si_{0.4}$(Pt)/Si(100) structure is a suitable candidate for the growth of NiSi layer in nanometric contacts that can be used for future device applications.

4. CONCLUSIONS

The electrical, crystalline and surface properties as well as the thermal stability of NiSi nanolayers formed by a solid state reaction of the co-sputtered Ni(Pt 4at.%) and $Ni_{0.6}Si_{0.4}$(Pt 4at.%) films grown on Si(100) substrates were studied. It was shown that these physical properties can be affected by changing annealing temperature in a long time and addition of Si to the deposited Ni layer. For the Ni(Pt)/Si structure, agglomeration of the grains as well as the degradation of its thermal stability were observed at low temperature (500°C). Instead, in the $Ni_{0.6}Si_{0.4}$(Pt)/Si structures, crystalline NiSi layer with lower R_s value of ~ 4 Ω/ is formed and it shows more thermal stability in the temperature range of 400-900°C. The knowledge obtained through this study can be applied for controlling the thermal stability as well as the surface morphology of the NiSi layer, e.g thermally stable NiSi layer with a typical surface roughness less than 8 nm obtained in the $Ni_{0.6}Si_{0.4}$(Pt)/Si structure is suitable material as a contact layer for future device fabrications at nano scale.

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