Int. J. Nanosci. Nanotechnol., Vol. 9, No. 1, March 2013, pp. 15-24

Optimized Design of Multiplexor by Quantum-dot Cellular Automata

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(Received:02 Nov. 2012 and Accepted: 28 Feb. 2013)

Abstract:
Quantum-dot Cellular Automata (QCA) has low power consumption and high density and regularity. QCA widely supports the new devices designed for nanotechnology. Application of QCA technology as an alternative method for CMOS technology on nano-scale shows a promising future. This paper presents successful designing, layout and analysis of Multiplexer with a new structure in QCA technique. In this paper we generalize a 2 to 1 multiplexer, which is used as module to implement the 2^n to 1 multiplexer. In this paper, we will present successful simulation of the 2 to 1, 4 to 1 and 8 to 1 multiplexer with QCA Designer. We will design a new multiplexer based on the majority gate with the minimum number of cells and consumed area. Being potentially pipeline, the QCA technology calculates with the maximum operating speed. We may use these multiplexers in the FPGA and ALU.
Keywords: *Majority gate, Module, Multiplexer, Quantum-dot cellular automata(QCA).*

1. INTRODUCTION

QCA as a well-known technology is able to replace devices based on FET (Field Effect Transistor) on nano-scale. Dominant scaling in CMOS has encountered some restrictions after some decades. This has led to fast development of molecular devices in nano-scale. QCA is a promising example in nanotechnology. In QCA, binary data appear as loading quantum-dots within the cells. Numerous studies are reported in which QCA is able to produce devices with high density, low power consumption and very high switching speed.
QCA was first proposed by Lent *et.al*, in 1993 and was developed in 1997. It is expected that QCA will play an important role in nanotechnology research. Due to significant features of QCA, high concentration, low consumer power, very high processing potential and being pipeline, it has become an interesting alternative for CMOS technology. Using molecular QCAs, we can have a concentration higher than 1000 devices per cm^2 and a performance faster than 2.5THz. Theoretically, processing speed may reach 25THz.
Several QCA multiplexer designs have been proposed [9-11]. Mardiris et al. [9,10] present the design of novel design of a quantum-dot cellular automata (QCA) 2 to 1 multiplexer. A module design and simulation methodology is developed, which can be used to design 2^n to 1 QCA multiplexers using the 2 to 1 QCA multiplexer as a building-block [10].
To meet this specification, the design must be consisted of elementary blocks properly selected so that it can be used to build larger 2^n to 1 multiplexers. The design includes an AND block, an (a•b) AND block and an OR block. It also includes one signal delay block at the i1 input of the circuit. All blocks are colored according to the clock they use. In the case of QCA, the multiplexer is pipelined. Each of the multiplexers [10], has an inordinate latency and very complex circuit.

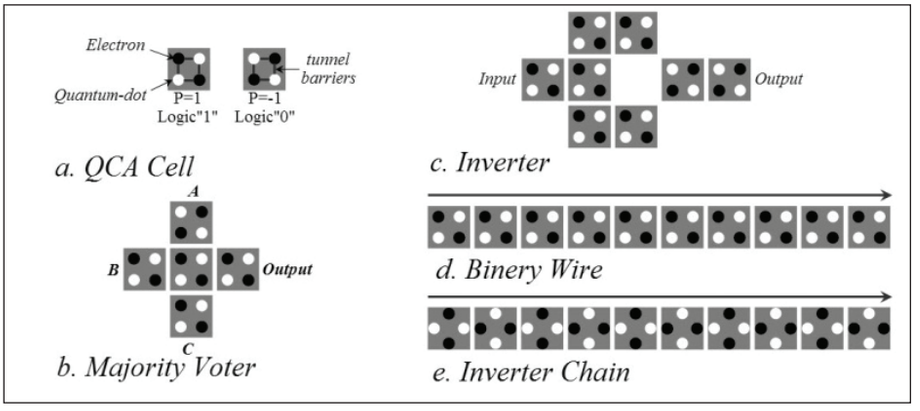


Figure 1: *Basic QCA logic devices.(a) QCA cell, (b)Majority voter(MV), (c) Inverter, (d)Binary wire, (e)Inverter chain.*

Kianpour et al. [11] have implemented a 4 to 1 multiplexer with five-input majority gate. For the 8 to 1 multiplexer, the authors use two 4 to 1 multiplexer. As a result, a given input signal traverses several clock zones before reaching the input of the logic block. Thus, significant latency is contributed by interconnection.

In this paper, we concentrate on designing, implementing and analyzing a basic device in QCA and use it in one of the most fundamental circuits in QCA. Designing method in QCA is different from that of CMOS, so that we will use quantum cells in QCA as transistor in CMOS technology. Here, we will present a new design of 2 to 1 multiplexer with minimum number of cells, delay and complexity.

This 2 to 1 multiplexer is used in designing 4 to 1, 8 to 1 multiplexer and finally the 2 to 1 multiplexer is used as module, to implement the 2^n to 1 multiplexer. We follow two objectives in our designs: 1. Implementation with the minimum complexity and number of cells; 2. Simplification of connections, decreasing delays and consequently increasing processing speed.

This paper is organized as follows: Section II reviews the QCA. In Section III, the design and implementation of the multiplexer are shown. In section IV, multiplexer implementation in QCA is presented. In section V, simulation results are shown. Conclusions are given in the last section.

2. QCA REVIEW

2.1. Background

QCA technology shows a promising future with a new view about designing circuits at nano-scale. The main unit of QCA is QCA cells located on the vertices of a square by four quantum-dots. A QCA cell includes four quantum dots on four vertices of a square having two electrons moving by tunneling between quantum dots. Due to Coulomb interaction, the electrons will only be located on the square diameter producing two polarizations as shown in Figure 1(a).

QCA functions based on coulomb interaction that transfers the state of one cell to another connected cell. The efficiency of QCA cells based on particular patterns can be dependent on the ground state of the system based on a logical function. Basic logical devices are for majority voter and inverter gates. The logical function of majority gate is as follows:

F (A,B,C)= AB+AC+BC

Where A, B and C are our inputs and F is our output and the cell in the center is the main cell. In Figure 1(b), we have indicated the majority gate with three inputs and in Figure 1(c), the inverter gate is presented. Binary wires and inverter chain are used for cross-over and array combinations in QCA circuits. Two types of wires are used in QCA technique. Figure 1(d) presents a 90 degrees binary wire and Figure 1(e) shows the inverter chain or 45 degrees wire [1-5].

2.2. QCA clocking

In VLSI systems, timing is controlled by a reference signal (a clock) needed for sequential circuits. Timing in QCA is performed by clocking at four consecutive and distinct phases which are necessary for both sequential and combinational circuits. Not only does clocking control the information flow but also supplies the real power in QCA. Clocking in QCA includes four phases: switch, Hold, Release and Relax as shown in Figure 2(a).

Cells in each zone perform a particular calculation. During Relax phase, electrons are pulled into the middle dots so that the cell is in null state. During Switch phase, internal barriers of dots slowly raise up and press the electrons between the corners so that the affected cell reaches the final polarization of the neighboring cell. During Hold phase, the barriers are up and the cell remains in polarization and affects its neighbor. Finally, during Release phase, the barriers are down and the electrons are pulled into the middle dots so that the cells lose their polarization [6-8].

3. PROPOSED 2 TO 1 MULTIPLEXER IN QCA

The 2 to 1 multiplexer presented in this paper, with three majority gates has been implemented, which we used as two-input AND gate and OR gate with fixed one of inputs. In general, an electronic multiplexer allows a system to select one of the several input signals and forward it to the output.

3.1. Logical 2 to 1 multiplexer in QCA

The 2 to 1 multiplexer in the first component uses two 2-input AND gates. The inputs of AND gates are connected to the selector wire S, and the inputs In1 and In2 lines through inverter gates needed as shown in Figure 3. The 2 to 1 multiplexer in the second component uses one 2-input OR gates. In QCA technology, each logic gate with more than three inputs is built by cascading multiple 3-input gates. The logical functionality is as follows: If the S rails are “0 or 1”, the outputs are setting with “In1or In2” sequentially.

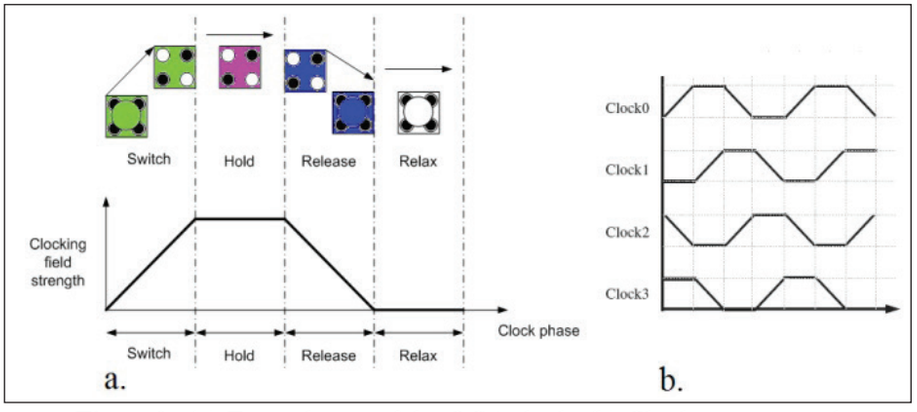
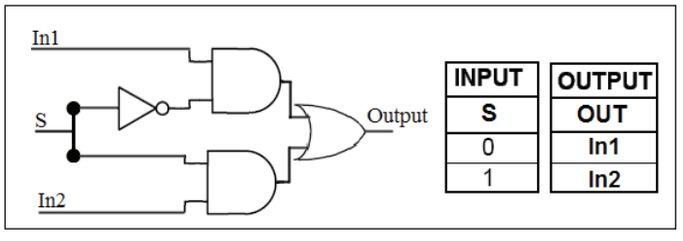


Figure2: *(a) Four phases of the QCA clock, (b) Clock zones signal.*



INPUT	OUTPUT
S	OUT
0	In1
1	In2

Figure 3: *Schematics for 2 to 1 multiplexer with truth table.*

Figure 4 shows a 2 to 1 multiplexer implemented in QCA with conventional gates.

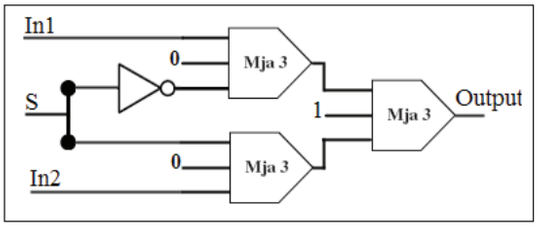


Figure 4: *A 2 to 1 multiplexer implemented in QCA.*

3.2. Implementation and simulation result of proposed 2 to 1 multiplexer in QCA

The circuit is designed and simulated for functional behavior using the QCA Designer Ver. 2.0.3. In the bistable approximation, the following parameters were used: Number of samples = 50000, Convergence tolerance = 0.001, Radius of effect = 65nm, Relative permittivity = 12.9, Clock high = 9.8e-022, Clock low = 3.8e-023, Clock shift = 0, Clock amplitude factor = 2, Layer Separation=11.5, Maximum iteration per sample = 100.

The proposed 2 to 1 multiplexer consists of 22 cells covering an area of 0.03μm^2. Figure 5 shows layout of a 2 to 1 multiplexer by QCA techniques presented in this paper. The simulation results of the 2 to 1 multiplexer are presented in Figure 6. Two waveforms with different frequencies are applied at the inputs In1 and In2, and the multiplexer outputs the signal at In1 when the select signal S is low and outputs the signal at In2 when select signal S is high. The result, the multiplexer is an extremely important part of signal control systems, because it allows the system to choose one of the several inputs to be forwarded to the output. As it is observed, delay in this implementation is 3/4 clock cycle (three phases).

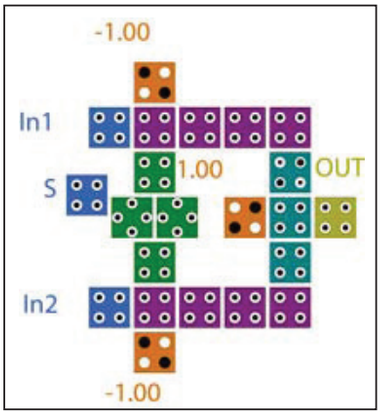


Figure 5: *A 2 to 1 multiplexer layout in QCA.*

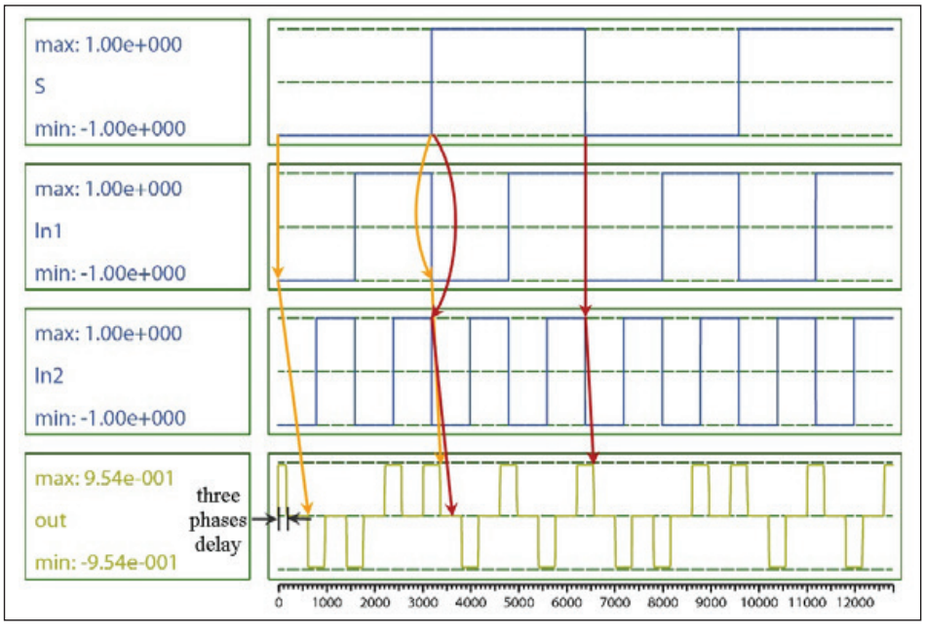


Figure 6: *The simulation results of 2 to 1 multiplexer.*

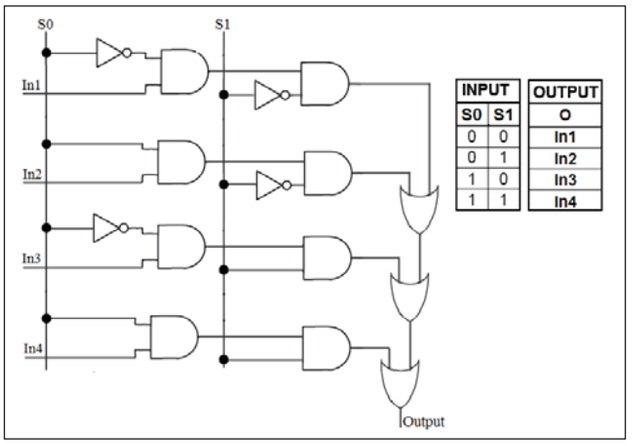


Figure 7: *Schematics for 4 to 1 multiplexer with truth table.*

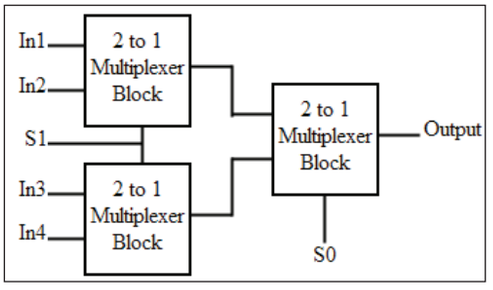


Figure 8: *Schematics of 4 to 1 multiplexer by 2 to 1 multiplexer module block.*

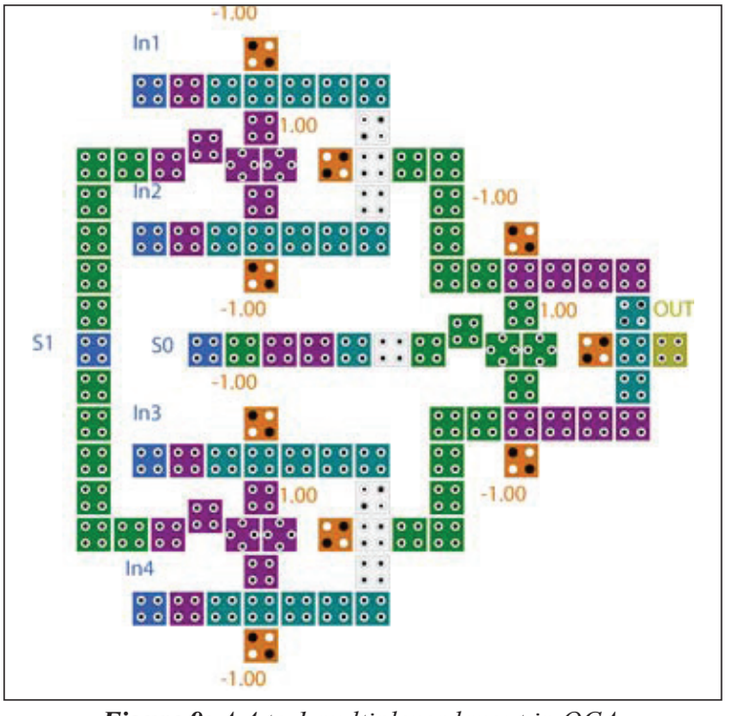


Figure 9: *A 4 to 1 multiplexer layout in QCA.*

4. 2^N TO 1 MULTIPLEXER IMPLEMENTATION IN QCA

In this article, we have designed a hierarchical circuit. First, we designed a 2 to 1 multiplexer and then with connection of three 2 to 1 multiplexer we produced the 4 to 1 multiplexer circuit. Finally, the 8 to 1 circuit is made by linking seven 2 to 1 multiplexers. Generalizing these 2 to 1 multiplexers proposed only requires a connection circuit; Hence, the 2 to 1 multiplexer is used as module, to implement the 2n to 1 multiplexer.

4.1. Implementation and simulation result of proposed 4 to 1 multiplexer in QCA

The 4 to 1 multiplexer in the first-stage uses four 2-input AND gates. The inputs of AND gates are connected to the input wire A, and the inputs In1,…,In4 through inverter gates needed as shown in Figure 7. The 4 to 1 multiplexer in the second-stage uses seven 2-input gates. Four of seven 2-input gates are used to AND input wire B with first-stage outputs. Furthermore, three of seven 2-input gates are used to OR second-stage output together. In Figure 7, the circuit configuration is the same as in the two stages multiplexer with eight 2-input AND gates and three 2-input OR gates. The logical functionality is as follows: If the S0, S1 rails are "00, 10, 01, 11", the outputs are setting with "In1, In2, In3, In4" sequentially.
The same logic 4 to 1 multiplexer that was depicted in Figure 7, is implemented by employing 2 to 1 multiplexer module block. Figure 8 represents the 4 to 1 multiplexer implementation in the QCA.
The proposed 4 to 1 multiplexer consists of 104 cells covering an area of 0.14 μm^2. Figure 9 shows layout of a 4 to 1 multiplexer by QCA. As illustrated in Figure 9, the complexity and delay will be reduced. The simulation results of the 4 to 1 multiplexer are presented in Figure 10. The inputs are In1, In2, In3, In4 and the selection lines are S0 and S1. Based on the Selection inputs S0 and S1, the multiplexer produces the output from the respective four inputs. In general, the number of 2 to 1 multiplexers required to design any higher order multiplexers is "n-1", where 'n' is the number of inputs of the multiplexer. In this case, we are designing a four input multiplexer and therefore, we require three 2 to 1 multiplexers. As the simulation result is observed, delay in this implementation is 1.75 clock cycle (seven phases).

4.2. Implementation and simulation result of proposed 8 to 1 multiplexer in QCA

As noted above, 2 to 1 multiplexer presented in the previous section can be considered as a module, which has a fixed structure and the correct clocking. In this section can be seven of these modules to put together, and with good connections to build an 8 to 1 multiplexer. The module block diagram of the 8 to 1 multiplexer is as shown in Figure 11. Figure 12 demonstrates an 8 to 1 multiplexer by QCA techniques presented in this paper. Here, In1 to In8 are the inputs of the multiplexer and S0, S1 and S2 are the select lines of the multiplexer. The proposed 8 to 1 multiplexer consists of 312 cells covering an area of 0.39 μm^2. The simulation results of the 8 to 1 multiplexer are presented in Figure 13. As the simulation result is observed, delay in this implementation is 2.5 clock cycle (ten phase).
Generalizing these 2 to 1 multiplexer provided only requires a driver circuit. In general, the number of 2 to 1 multiplexers required to design any higher order multiplexer is "n-1", where 'n' is the number of inputs of the multiplexer. For example, if we want a 16 to 1 multiplexer implementations, we need fifteen 2 to 1 multiplexers. This 16 to 1 multiplexer will attain the output in the thirteen clocks phase.

5. SIMULATION RESULT

In our design we used QCADesigner Ver. 2.0.3 in the bistable approximation. Table I, presents a brief description for each parameter used for a simulation engine.
In Table II, we made a comparison of area (μm^2), complexity (number of cells), delay (10^{-12}s in 1THz), power consumption and number of majority gates used in multiplexers.
Lent has mentioned in [1],[12] that power

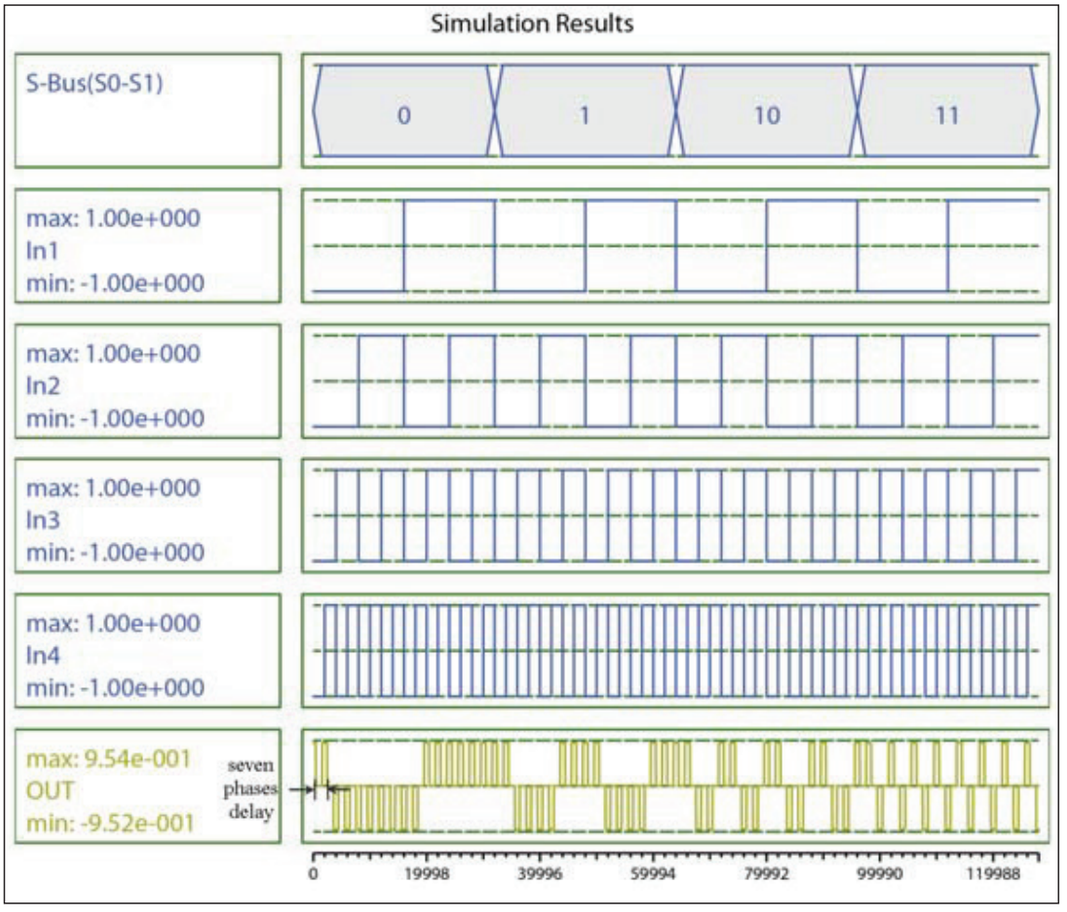


Figure 10: *The simulation results of 4 to 1 multiplexer.*

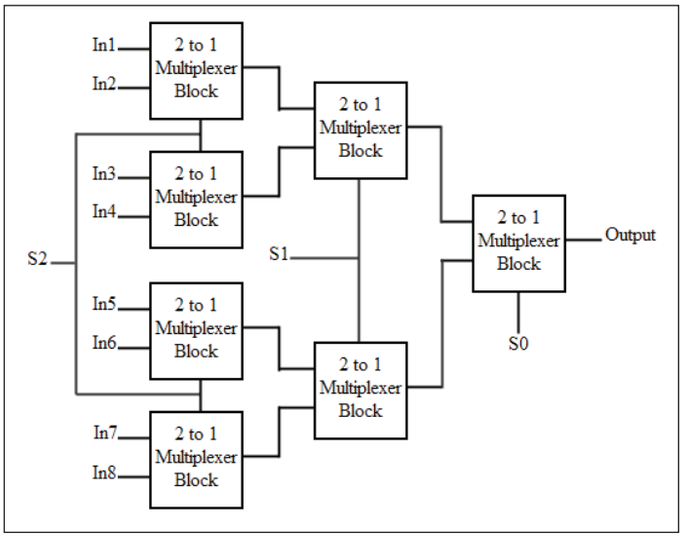


Figure 11: *Schematics of 8 to 1 multiplexer by 2 to 1 multiplexer module block.*

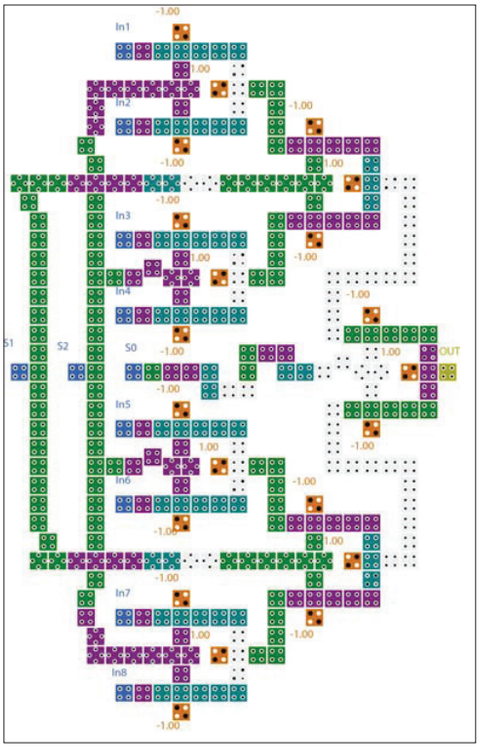


Figure 12: *A 8 to 1 multiplexer layout in QCA.*

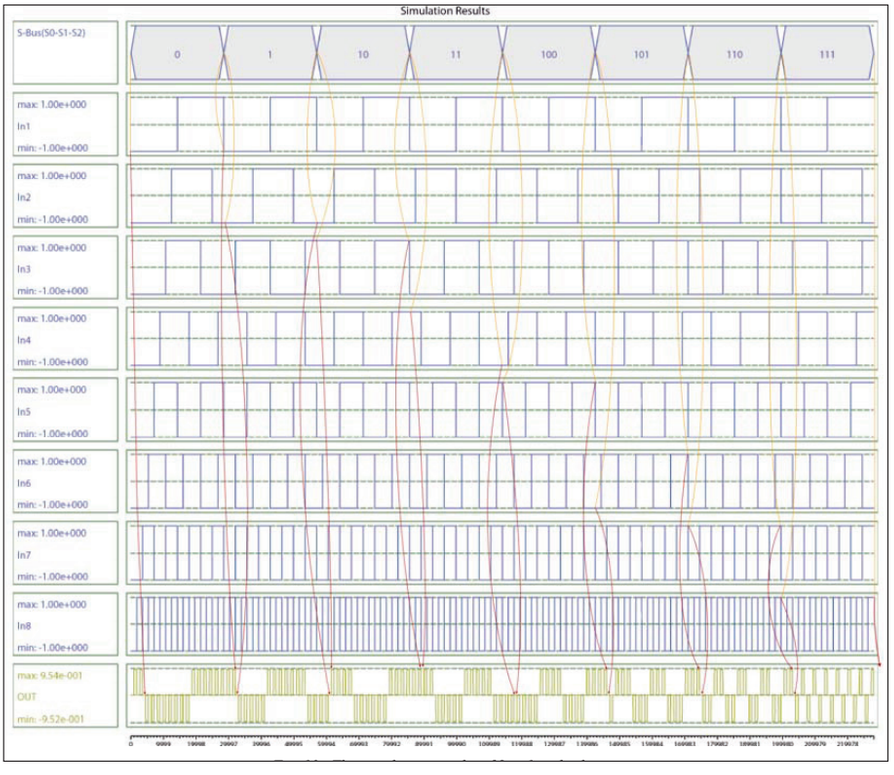


Figure 13: *The simulation results of 8 to 1 multiplexer.*

consumption in QCA arrays is 10^{-10}W per input bit nearly; therefore, in 4-bit designs, power consumption will be 4×10^{-4} μW. This assumption can be used to calculate the approximate power consumption of the circuits designed in this paper. Results can be seen in Table II.

Table I: *parameters model in qcadesigner simulator*

Parameter	Value
Cell width	18nm
Cell height	18nm
Dot diameter	5nm
Number of samples	50000 – 1000000
Convergence tolerance	0.001
Radius of effect	65nm
Relative permittivity	12.9
Clock high	9.8e-22J
Clock low	3.8e-23J
Clock amplitude factor	2
Layer Separation	11.5nm
Maximum iteration per sample	100

6. CONCLUSION

We presented a new design of 2 to 1 multiplexer in the QCA, which could achieve a high efficiency. In each section we explained the application of 2 to 1 multiplexer in designing and implementing 4 to 1 and 8 to 1 multiplexers. The modularity of the design method allows the determination of the number of QCA cells and the covered area for the 2n to 1 QCA multiplexers. These new multiplexers compared to previous works significantly improved area, complexity, delays and power consumption. We can use these multiplexers in processors with high operating speed and this circuit is applicable in the core of high-speed FPGA and ALU processors.

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Table II: *Comparison between multiplexers presented in this paper and previous work in [10],[11]*

	2 to 1 Multiplexer			4 to 1 Multiplexer			8 to 1 Multiplexer		
	proposed in this paper	Design proposed by [10]	Design proposed by [11]	proposed in this paper	Design proposed by [10]	Design proposed by [11]	proposed in this paper	Design proposed by [10]	Design proposed by[11]
Area (μm^2)	0.03	0.07	unknown	0.14	0.24	0.17	0.39	0.67	0.49
Complexity (# Cell)	22	56	unknown	104	215	229	312	633	679
Delay (10^{-12}s in 1 THz)	0.75	1	unknown	1.75	1.75	2.75	2.5	3	5.75
Power (μW)	3×10^{-4}	unknown	unknown	12×10^{-4}	unknown	unknown	22×10^{-4}	unknown	unknown
Number of three-input majority gate	3	3	unknown	9	11	3	21	31	15

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