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# Static Simulation of CNTFET-based Digital Circuits

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***Abstract***
*In this paper we implement a simple DC model for CNTFETs already proposed by us in order to carry out static analysis of basic digital circuits. To verify the validity of the obtained results, they are compared with those of Wong model, resulting in good agreement, but obtaining a lighter ensuring compile and shorter execution time, which are the main characteristics to have an easy implementation in circuit simulators for CAD applications.*
***Keywords:*** *CNTFET, Digital design, Static analysis.*

## 1. INRODUCTION

The evolution of electronics has been possible thanks to a scaling operation ever progressing with the time. This scaling evolution has been described by the Moore's law, which states that in an integrated circuit the number of transistors doubles every 18 months.

However, today the scaling operation of silicon devices is saturated since these devices cannot be more shrunk without degrading their performances for the arising of some phenomena like tunnel effects [1] or the perforation of the gate oxide also for voltages relatively low.

Therefore, the scientific community is looking for a new kind of devices, able to work better at nanometer scale, which is the new frontier.

Along with these new devices, molecular electronics will change the equation in our tool box, we will drop out well known partial differential equation for charge diffusion and we will use quantum mechanics to describe electrons, holes, atoms, molecules and photons. In coming years we will gain new tools from chemistry and physics, new sophisticated mathematical tool including probability amplitude waves.

Carbon NanoTube Field Effect Transistors (CNTFETs) are a new kind of molecular device and are regarded as an important contending device to replace conventional silicon transistors [2-4].

One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [2-3].

As it is known, the carbon nanotubes consist in a hexagonal mesh of carbon atoms wrapped in cylinder shapes, some time with closing hemispherical meshes on the tips. These tubes could have various radii, lower than two nanometres and, since they could be extended several millimetres, they have a huge length/diameter ratio making them unidimensional structures. Depending on the mesh torsion, denoted as *chirality*, electronic band structure of CNT

changes, band gap may appear making them semiconductors, or may not appear, making them conductors [5-6].

Furthermore the CNT behaviour as semiconductor has an energy gap inversely proportional to their radius.

About modelling issues, the research on CNTFETs has proposed various models available in literature, which are numerical and make use of self-consistency and therefore they do not allow an easy implementation in circuit simulators (SPICE, Verilog-A or VHDL-AMS), which instead must be the main characteristic in the field of Computer Aided Design (CAD).

In [7-14] we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A.

In this paper we implement our CNTFET model to carry out static analysis of basic digital circuits.

In order to verify the validity of the obtained results, they are compared with those of Wong model [15-16], resulting in good agreement.

However our model allows significant improvements compared to Wong model, because we have obtained a lighter ensuring compile and shorter execution time, without losing in accuracy, which are the main characteristics to obtain an easy implementation in circuit simulators.

The presentation is organized as follows. At first we briefly describe our DC CNTFET model. Then we show the analysis of some logic gates and discuss the relative results, together with conclusions and future developments.

## 2. A REVIEW OF THE EXAMINED DC MODELS

An exhaustive description of our DC model is in [6] and [11]. In this section we just describe the main equations on which is based our model.

Figure 1 shows a 3D representation of a C-CNTFET [6], whose conduction behaviour is similar to a common MOSFET.

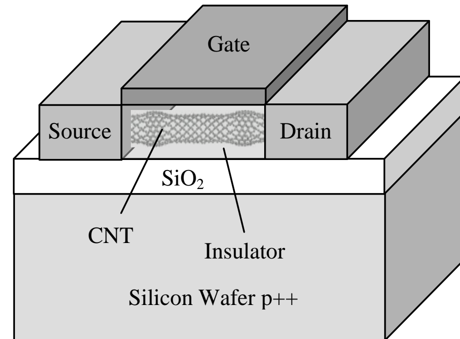



***Figure 1.*** *3D representation of a C-CNTFET.*

When a positive voltage is applied between drain-source ($V_{DS} > 0$ V), the previous hypothesis allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source ($V_{GS} > 0$ V), the conduction band at the channel beginning decreases by $qV_{CNT}$, where $V_{CNT}$ is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [17]:

$$I_{DSp} = \frac{4qkT}{h}\left[\ln\left(1+\exp \xi_{Sp}\right) - \ln\left(1+\exp \xi_{Dp}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while $\xi_{Sp}$ and $\xi_{Dp}$ have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT}$$

and (2)

$$\xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT}$$

being $E_{Cp}$ the sub-bands conduction minima.

Therefore the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h} \sum_{p} \left[ \ln\left(1 + \exp \xi_{Sp}\right) - \ln\left(1 + \exp \xi_{Dp}\right) \right] \quad (3)$$

The surface potential, $V_{CNT}$, is evaluated by the following approximation:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \frac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \frac{E_C}{q}\right) & \text{for } V_{GS} \geq \frac{E_C}{q} \end{cases} \quad (4)$$

where $E_C$ is the conduction band minimum for the first sub-band.

The parameter $\alpha$, depending on $V_{DS}$ voltage, CNTFET diameter and gate oxide capacitance $C_{ox}$, has been extracted from the experimental device characteristics [7].

In the following simulations, our model has been translated in the programming language Verilog [18] and then implemented on the simulator Advanced Design System (ADS).

The Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET) [15-16], named by us as *Wong model*, is the development of the previous one, known in literature as Stanford CNFET model (S-CNFET) [19-20].

The VS-CNFET model is based on the semi-empirical virtual source concept calibrated to experimental data.

In particular the intrinsic drain current and terminal charges are based on the virtual source (VS) model, with the virtual source velocity extracted from experimental data for different channel lengths (ranging from 3-um down to 15-nm).

Moreover the VS-CNFET model takes in account the following parasitic effects:

1. direct source-to-drain and band-to-band tunneling current calibrated by numerical simulations;
2. metal-to-CNT contact resistances calibrated by experimental data;
3. parasitic capacitance including gate-to-CNT fringe capacitances and gate-to-contact coupling capacitances.

The inputs to the VS-CNFET model are the physical device design including device dimensions, CNT diameter, gate oxide thickness, etc.

## 3. STATIC ANALYSIS OF CNTFET LOGIC GATES

### 3.1. Logic Gate Parameters for Static Analysis

Referring to an inverter, for a static analysis we can determine the voltage transfer characteristic, VTC (Figure 2), and then the noise margins, which provide a measure of the maximum external voltage noise that can be overlapped to the input signals, without causing unwanted output variation.

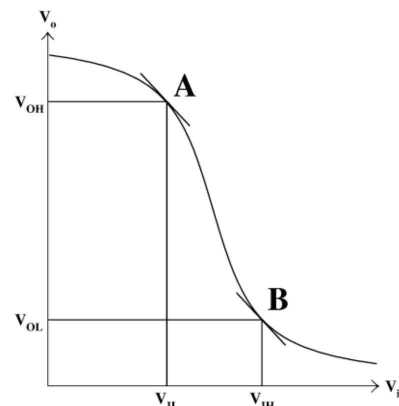



***Figure 2.*** *Voltage transfer characteristic for an inverter.*

The noise margins, whose values are necessary in the design of digital circuits, are determined from the -1 slope points on the VTC, indicated by the letters A and B in Figure 2, which delimit the amplification range of the device. $V_{OH}$ and $V_{IL}$ (point A) represent respectively the valid minimum

output voltage at high level and the valid maximum input voltage at low level. Similarly $V_{OL}$ and $V_{IH}$ (point B) the valid maximum output voltage at low level and the valid minimum input voltage at high level.

The noise margins are defined as follows:

$NM_H = V_{OH} - V_{IH}$ for high voltage
and (5)
$NM_L = V_{IL} - V_{OL}$ for low voltage.

When the input voltage $V_I$ is between $V_{IL}$ and $V_{IH}$, the logic gate is in an undefined state, which is an operative condition that we must avoid to make sure the logic levels are within well defined regions.

**3.2 Static Analysis of NOT Gate**

The schematic of a NOT gate implemented by Verilog-A language is shown in Figure 3.

The gate consists of two MOS-like CNTFETs with n and p channel respectively.

In Figure 3 Gate-in and Out indicate the input and the output of the gate, while V+ and V- indicate the positive and negative power supply terminals. Two current probes have been introduced to evaluate static currents flowing through the two CNTFETs.

Finally, two capacitors have been introduced to model the capacitance of the metallic interconnections with respect to ground, which have no influence in static performance, but in dynamic analysis are important for new measurement technology. By using switching methods, it is important shorter execution time for each switching state [21-22].

In order to perform a static analysis, we have used the circuit reported in Figure 4, which shows a cascade of five NOT gates, which are internally composed as in Figure 3. A dual power supply is used and a constant voltage source $V_{in}$ is connected to the input of the first gate and varies from $-V_{CC}$ to $+V_{CC}$ ($V_{CC}$ varies from 0.1V to 1V with step 0.1V).

The VTCs of the first NOT gate of the cascade are determined both with the proposed model and with Deng-Wong model, in order to compare them.

We have observed how increasing the supply voltage increases the logic swing of the output voltage $\Delta V = V_H - V_L$. Moreover, with Wong model [15-16], ADS reports some convergence problems for $V_{CC} \geq 0.5V$, while in our model these problems are absent.

Moreover, for the proposed model, increasing the voltage supply, the slope of the characteristics in the high gain region decreases, while this effect is less evident for Wong model.

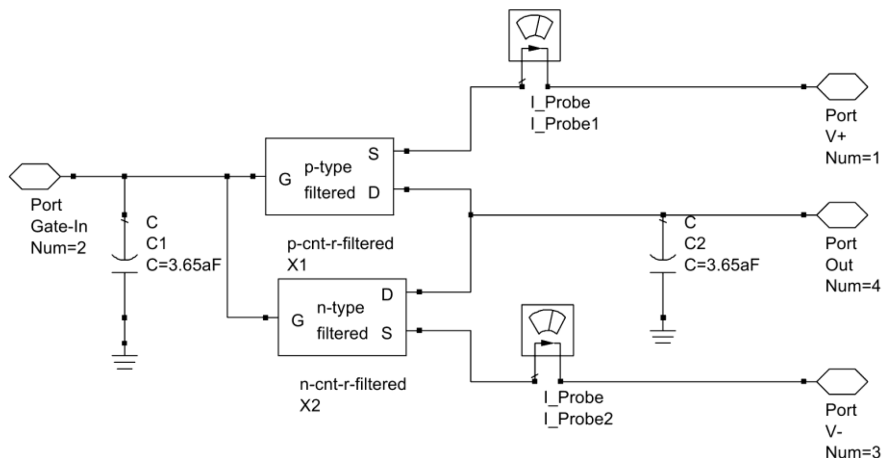



***Figure 3**. Schematic of a NOT gate.*

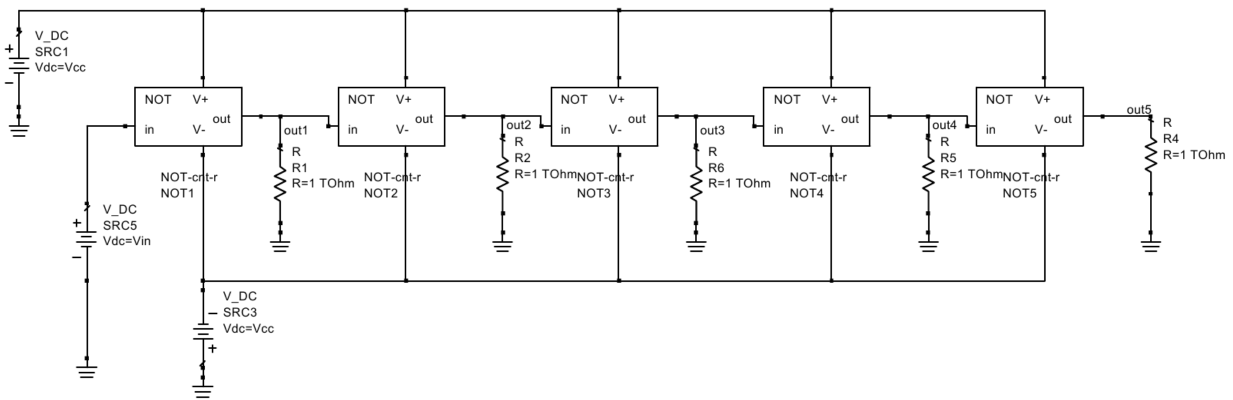
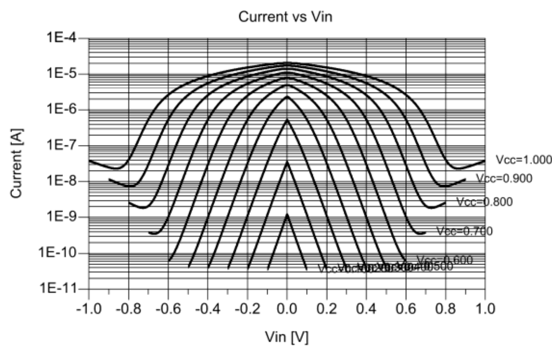
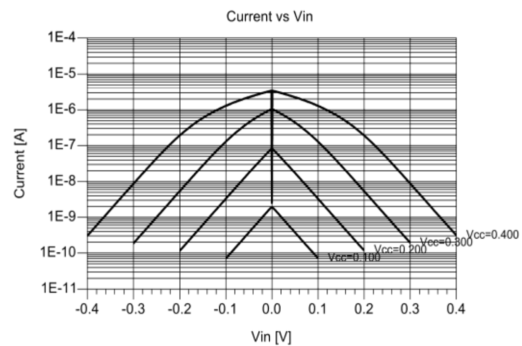



*__Figure 4__. Schematic of a cascade of five NOT gates.*

In Figure 5(a) and 5(b) we have reported the simulated static currents of the first gate of the cascade with the proposed and Wong models respectively. These currents give an indication of the static power dissipation in the circuit, which is a very important factor for high integration density circuits.




(a)




(b)

***Figure 5**. (a) Static currents of the first NOT gate vs $V_{in}$, with $V_{CC}$ varying from 0.1 V to 1.0 V, step 0.1 V (our model); (b) the same, with $V_{CC}$ varying from 0.1 V to 0.5V, step 0.1 V (Wong model).*

Current peacks in the high gain region (near $V_{in}$ = 0 V) are to be observed, because in this region the two CNTFETs of the NOT gate are both in the on state and they are saturated. A conducting path between the positive and negative power supply is determined and relatively high currents can flow. We can see in the figures that the current decreases in the regions where the gate state is well defined, i.e. the states where the input signal is recognized as low or high level. In these regions, where one transistor is turned on and the other one is turned off, the static current that flows between the positive and negative supply is due to the tunnel effect in the interdicted transistor.

As we said previously, noise margins are determined from the -1 slope points on the VTC. This slope is the gate gain, defined as $\frac{\partial V_{out}}{\partial V_{int}}$, and can be determined using the circuit of Figure 6.

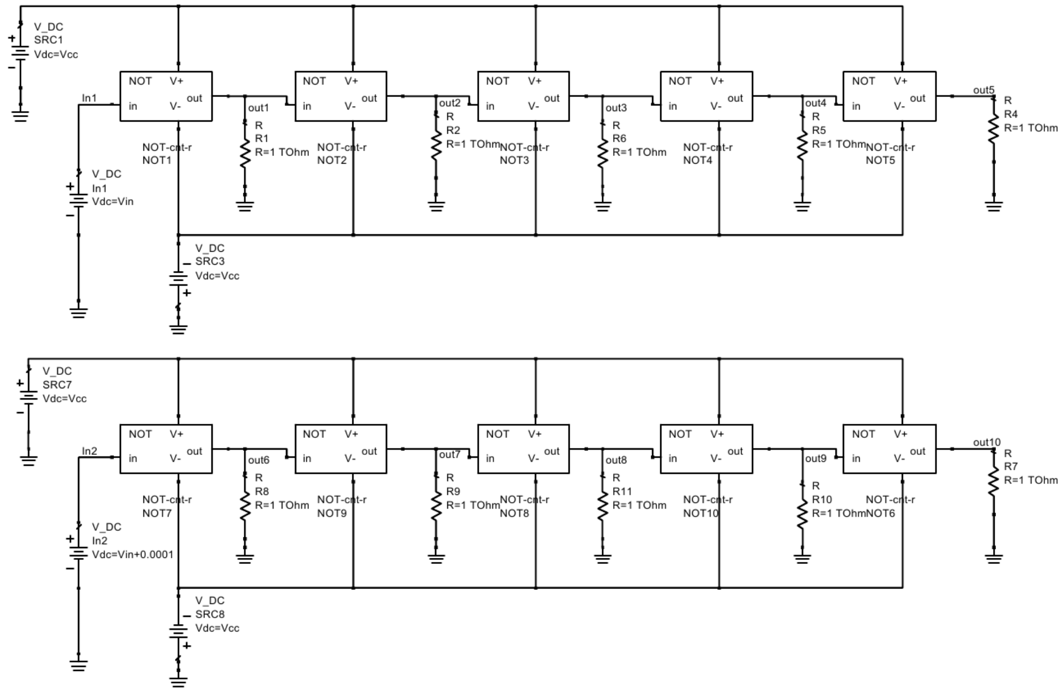



***Figure 6.*** *Circuit used to calculate NOT gain.*

In particular Figure 6 shows two identical circuits in which the lower one presents an input voltage increased by $\Delta V_{in}$ = 0.1mV with respect to the upper circuit. Referring to the first gate of the cascade, considering the difference between the outputs of the lower and upper circuit and dividing that by $\Delta V_{in}$ we obtain the gate gain:

$$\frac{\partial V_{out}}{\partial V_{in}} \cong \frac{\text{out6} - \text{out1}}{\text{In2} - \text{In1}} \qquad (6)$$

where out1 and out6 are the outputs of the first gate of the cascade referring to the upper and lower circuit, whereas In1 and In2 are the inputs of the first gate of the upper and lower circuit respectively.

In this way we can obtain the gain diagrams of NOT1 gate as function of input voltage for both models

Considering our model we saw that it turns out that, for $V_{CC}$ > 0.7 V, the gain has a non-monotone trend for 0.1V < $|V_{in}|$ < 0.4V which determines a double passage to the -1 value. This behavior could be used to create a multilevel logic, but in our case represents a situation to be avoided.

Similarly, plotting the gain as function of the output voltage of the first gate, we obtain $V_{OH}$ and $V_{OL}$, which are the output voltage values when the gain is -1.

In particular, in our model, for $V_{CC}$ > 0.7V the gain trend shows a double passage to the -1 value and therefore the voltage supplies considered are under this value.

At last, in Table 1, we have reported the $V_{IH}$, $V_{OL}$, $V_{IL}$, $V_{OH}$ values and the noise margins $NM_H$ and $NM_L$ for different values of $V_{CC}$ for our model, whereas in Table 2 the same for Wong model.

***Table 1.*** *Noise margins and -1 slope points (our model).*

| $V_{CC}$ (V) | $V_{IH}$(V) | $V_{OL}$ (V) | $V_{IL}$(V) | $V_{OH}$ (V) | $NM_H$ | $NM_L$ |
|---|---|---|---|---|---|---|
| 0.1 | 0.014 | -0.09 | -0.014 | 0.09 | 0.075 | 0,. 75 |
| 0.2 | 0.014 | -0.19 | -0.014 | 0.19 | 0.174 | 0.174 |
| 0.3 | 0.019 | -0.28 | -0.019 | 0.28 | 0.259 | 0.259 |
| 0.4 | 0.035 | -0.34 | -0.036 | 0.34 | 0.309 | 0.309 |
| 0.5 | 0.058 | -0.39 | -0.058 | 0.39 | 0.330 | 0.330 |
| 0.6 | 0.076 | -0.42 | -0.076 | 0.42 | 0.343 | 0.343 |
| 0.7 | 0.095 | -0.44 | -0.095 | 0.44 | 0.344 | 0.344 |

***Table 2.*** *Noise margins and -1 slope points (Wong model).*

| $V_{CC}$ (V) | $V_{IH}$(V) | $V_{OL}$ (V) | $V_{IL}$(V) | $V_{OH}$ (V) | $NM_H$ | $NM_L$ |
|---|---|---|---|---|---|---|
| 0.1 | 0.018 | -0.09 | -0.018 | 0.09 | 0.07 | 0.07 |
| 0.2 | 0.012 | -0.18 | -0.012 | 0.19 | 0.165 | 0.165 |
| 0.3 | 0.032 | -0.26 | -0.032 | 0.26 | 0.232 | 0.232 |
| 0.4 | 0.053 | -0.32 | -0.053 | 0.32 | 0.271 | 0.271 |

### 3.3 Static Analysis of NOR Gate

The schematic of the NOR gate is shown in Figure 7. The gate has five terminals, that are the two inputs (A-in and B-in), the output (out) and the positive and negative supply terminals (V+ and V-). The NOR consists of four CNTFETs (two n-channel and two p-channel), four capacitors modelling the interconnection-to-ground capacitances, three capacitors modelling the gate-to-gate and gate-to-drain parasitic capacitances of adjacent transistors and two current probes which we use to evaluate the currents flowing through the device in static or dynamic conditions. The interconnection-to-ground capacitances have been calculated considering the interconnection lengths equal to 50 nm. The gate-to-gate and gate-to-drain parasitic capacitances of adjacent CNTFETs have been estimated according to the value of 110 aF/µm proposed by Wong in [15-16]. However in static analysis these capacitances have no influence.

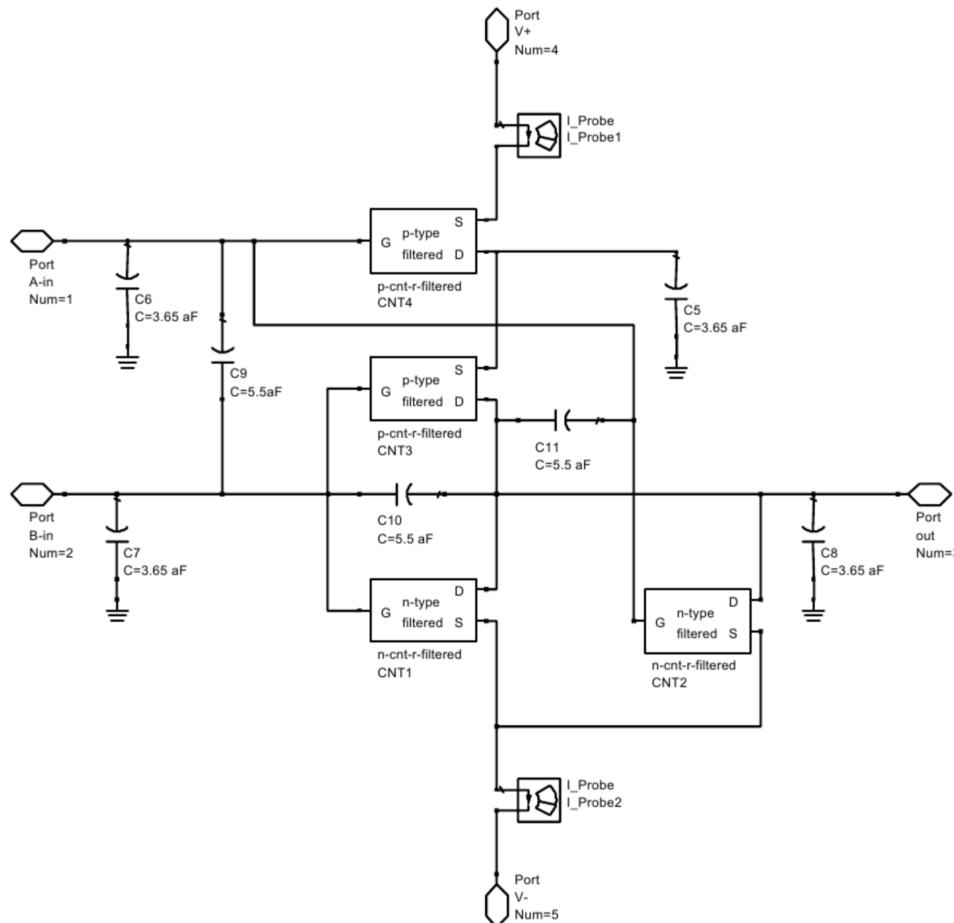



***Figure 7***. *Schematic of a NOR gate.*

Similarly to the NOT case, using CNTFETs implemented by Verilog-A, the proposed procedure has been applied to perform static analysis of a NOR cascade, whose schematic is shown Figure 8.

The circuit consists of two NOR gate in cascade, whose power supply terminals V+ and V- are respectively connected to $+V_{CC}$ and $-V_{CC}$. One input is maintained at a constant voltage value equal to $-V_{CC}$, whereas the other input is connected to a constant voltage source which varies, in the DC simulations, from $-V_{CC}$ to $+V_{CC}$ with step of 1mV.

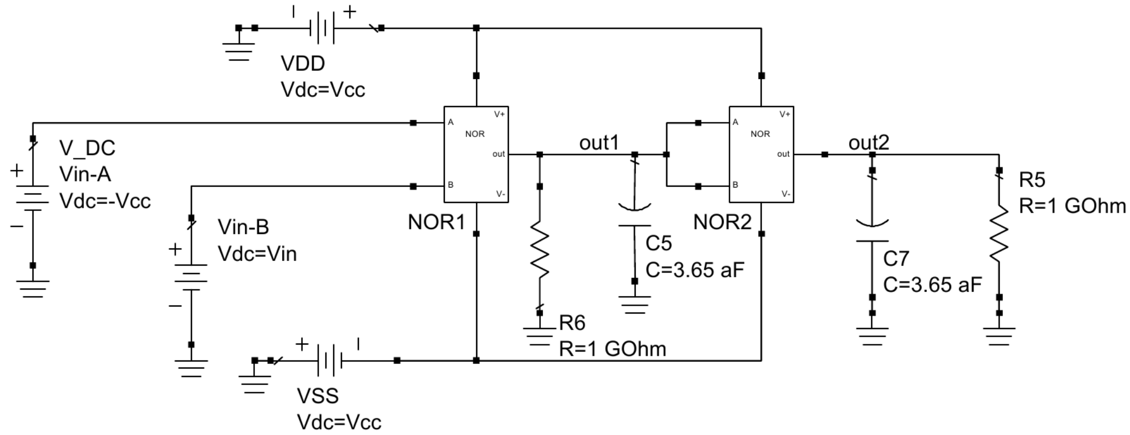



***Figure 8**. Schematic of NOR cascade.*

One of the NOR inputs is fixed to low level, so the gate works as an inverter for the signal going to the other input. The obtained VTCs show that for low level in input, the output is at high level and, similarly, for high level in input, the output is at low level, as expected. We also notice how the values of the output logic levels ($V_H$ and $V_L$) are determined by the supply values.

Also in this case we have calculated the static currents, obtaining with our model values greater than Wong model, because, considering the input voltages of Figure 8, the CNTFETs named as CNT1, CNT3 and CNT4 (Figure 7) are turned on, determining the presence of a conducting path between the positive and negative power supply.

Moreover we observe that the intensity of the current decreases corresponding to the region which indicate the well-defined states of the gate, where the input signal is recognized as a high or low voltage level. In this case the conducting path does not exist between the power supplies (contrary to the high gain region) and the currents which flow through the gate are the sub threshold CNTFETs currents [23-25].

In order to determine the noise margins of the NOR gate, as we have already illustrated for the NOT cascade, we must determine the noise margins considering the -1 slope points of the NOR VTCs. This slope is the gate gain, defined as $\frac{\partial V_{out}}{\partial V_{in}}$, and it can be obtained using the circuit in Figure 9.

In this figure we can observe two identical circuits of which the upper circuit presents an input voltage increased by $\Delta V_{in} = 0.1$ mV compared to the lower circuit. As we said before, one of the two inputs of the first gate of the cascade is maintained to low level, whereas the other varies from $-V_{CC}$ to $+V_{CC}$.

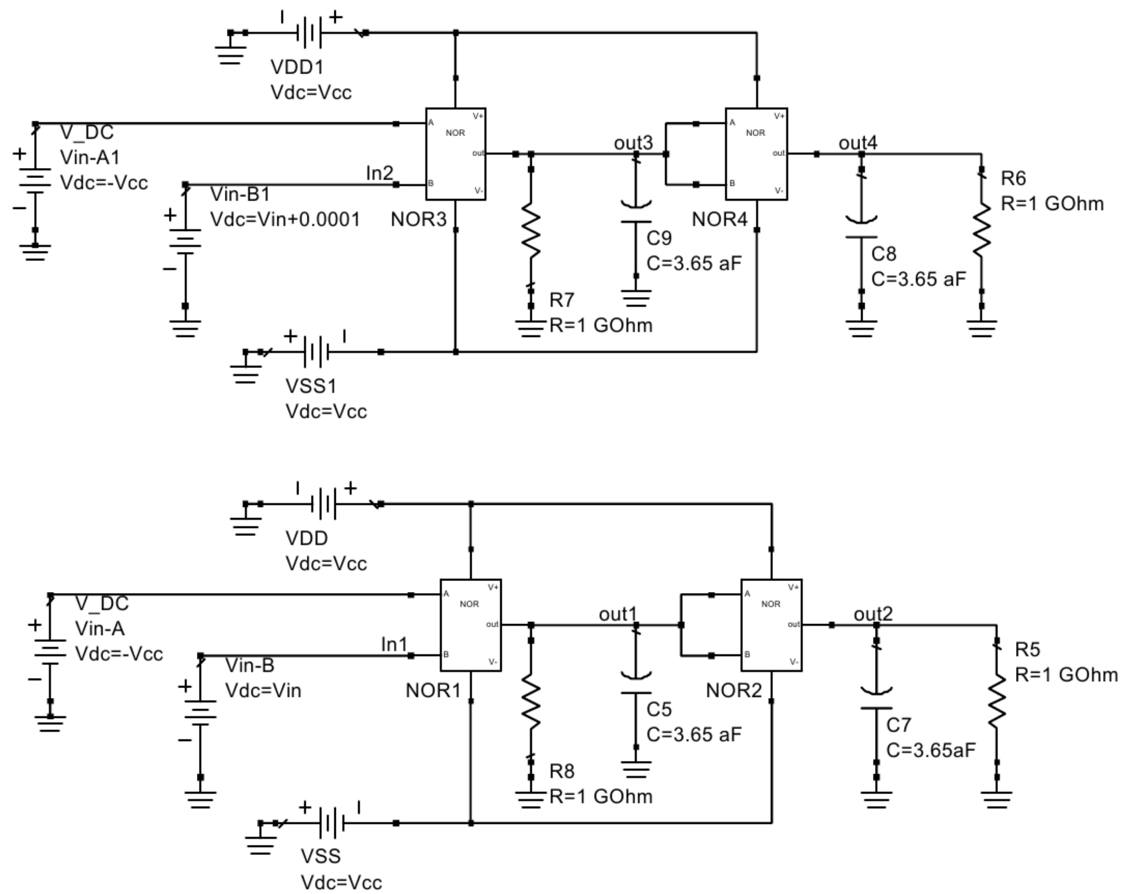



***Figure 9**. Circuit used to determine NOR gain.*

Referring to the first gate of the cascade, considering the difference between the output of the upper circuit and the output of the lower circuit and dividing that by $\Delta V_{in}$, we obtain the gate gain:

$$\frac{\partial V_{out}}{\partial V_{in}} \simeq \frac{\text{out3} - \text{out1}}{\text{In2} - \text{In1}} \qquad (7)$$

where out3 and out1 are the outputs of the first gate of the cascade which refer to the upper and lower circuit respectively, whereas In2 and In1 are the inputs of these gates referred to the upper and lower circuit.

For the NOR cascade, as for the NOT cascade, we determine the diagrams of the gain as function of the input voltage $V_{in}$ and the output voltage at the first gate, out1. The $V_{in}$ and out1 values corresponding to a gain equal to -1 will be extracted from the diagrams and, later, used in the noise margin calculation, as we have done for the NOT cascade.

In this way, as we have illustrated extensively for the case of NOT gate, we can obtain the simulations of the first gate gain as function of the input and output voltage, with the supply voltage as parameter, for both models. From these diagrams we can determine the -1 slope points of the transfer characteristics.

In order not to weigh the treatment, we limit ourselves to returning the values obtained. In particular, in Table 3 we have reported the $V_{IH}$, $V_{OL}$, $V_{IL}$, $V_{OH}$ values and the noise margins $NM_H$ and $NM_L$ for different values of $V_{CC}$ for our model, while in Table 4 the same for Wong model.

At last we would to say that all simulations were carried out in ADS 2014 on an Asus K55VD computer which uses an Intel Core i-7 3630QM processor running at

2.4 GHz, with 4 GB of RAM memory. Moreover we got 2.7 s and 58.8 s for the compilation time and run time respectively, versus 47.70 s and 1336.42 s of Wong model.

***Table 3.*** *Noise margins and -1 slope points (our model).*

| $V_{CC}$ (V) | $V_{IL}$ (V) | $V_{OH}$ (V) | $V_{IH}$ (V) | $V_{OL}$ (V) | $NM_H$ | $NM_L$ |
|---|---|---|---|---|---|---|
| **0,1** | -0,015 | 0,088 | 0,014 | -0,088 | 0,074 | 0,073 |
| **0,2** | -0,015 | 0,187 | 0,013 | -0,187 | 0,174 | 0,172 |
| **0,3** | -0,028 | 0,275 | 0,012 | -0,278 | 0,263 | 0,25 |
| **0,4** | -0,078 | 0,35 | 0,002 | -0,344 | 0,348 | 0,266 |
| **0,5** | -0,17 | 0,443 | -0,017 | -0,393 | 0,46 | 0,223 |
| **0,6** | -0,269 | 0,543 | -0,036 | -0,433 | 0,579 | 0,164 |
| **0,7** | -0,37 | 0,645 | -0,057 | -0,469 | 0,702 | 0,099 |
| **0,8** | -0,466 | 0,743 | -0,081 | -0,504 | 0,824 | 0,038 |

***Table 4.*** *Noise margins and -1 slope points (Wong model).*

| $V_{CC}$ (V) | $V_{IL}$ (V) | $V_{OH}$ (V) | $V_{IH}$ (V) | $V_{OL}$ (V) | $NM_H$ | $NM_L$ |
|---|---|---|---|---|---|---|
| **0,1** | -0,02 | 0,086 | 0,02 | -0,089 | 0,066 | 0,069 |
| **0,2** | -0,02 | 0,183 | 0,02 | -0,187 | 0,163 | 0,167 |
| **0,3** | -0,05 | 0,264 | 0,015 | -0,261 | 0,249 | 0,211 |
| **0,4** | -0,11 | 0,334 | 0 | -0,317 | 0,334 | 0,207 |
| **0,5** | -0,205 | 0,423 | -0,025 | -0,362 | 0,448 | 0,157 |
| **0,6** | -0,32 | 0,522 | -0,06 | -0,4 | 0,582 | 0,08 |
| **0,7** | -0,4 | 0,595 | -0,09 | -0,424 | 0,685 | 0,024 |

## 4. DISCUSSION OF RESULTS

In the light of the results obtained, for both models we observe symmetrical values of $V_{IH}$-$V_{IL}$ and $V_{OH}$-$V_{OL}$, because the n-channel and p-channel CNTFETs models and the circuit topology of the NOT gate are symmetrical.

As a consequence of this symmetry, for both models results that $NM_H = NM_L$.

For the NOR gate there is no symmetry for the $V_{IH}$-$V_{IL}$ and $V_{OH}$-$V_{OL}$ values. As a consequence, normally it results that $NM_H \neq NM_L$. For both models we obtain results that if the power supply value increases, the difference between $NM_H$ and $NM_L$ increases. So it is opportune to choose a not too large value of $V_{CC}$, in order to ensure homogeneous noise margins for both the high and low logic levels.

For the static analysis the two models have provided results that are in good agreement and the difference are mainly due to the greater differential output resistance presented by the Wong model in the saturation region of the CNTFET.

Moreover in [14] we have presented a comparison of two considered CNTFET models through the design of a 6T SRAM cell based on CNTFET. Also in this case the two considered models are almost equivalent in the design of a CNTFET SRAM, but for this application, our model is faster when using 16 cells, dissipates less power and is less affected by bitline noise during the writing operations. This result allowed us to say once again that our model seems to be particularly suitable for CAD applications [14].

## 5. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we have implemented a simple DC model for CNTFETs already proposed by us in order to carry out static analysis of basic digital circuits.

To verify the validity of the obtained results, they have been compared with those of Wong model, resulting in good agreement. However our model allows significant improvements compared to Wong model, because we have obtained a lighter ensuring compile and shorter execution time, without losing in accuracy, which are the main model characteristics to obtain an easy implementation in circuit simulators.

Actually we have implemented our CNTFET model, considering the capacity-ance effects, in order to carry out also dynamic and transient analysis of digital circuits, whose results will be described in a new article to be submitted as an extension of this paper.

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