Dual-V_{DD} System Design with Energy Efficient near-Threshold Voltage Level Converter

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Abstract

Multi-VDD design is one of the most effective lower-power design techniques. Multi-VDD VLSI circuits require voltage level converters to prevent high static power dissipation between different voltage islands. As the level conversion step imposes additional power and delay to the design, it is very important to optimize the level converter circuits for minimum power-delay product (PDP). This paper presents an energy efficient single supply level converter (SSLC) based on carbon nanotube FET (CNTFET) for near threshold dual-VDD circuits. CNTFET as an emerging nanotechnology is suitable for low-power and high-performance circuits design. The proposed SSLC is utilized in the structure of a modified low-power parallelized dual-VDD multiplier. Insertion of the proposed SSLC at the output stage of the multiplier significantly reduces static power and enhances the output driving capability. In the proposed SSLC, dynamically controlled source-body voltage reduces drain-induced barrier lowering (DIBL) effect. In addition, using dual-chirality CNTs leads to optimum static power and energy consumption. The simulation results, obtained using the Stanford CNTFET HSPICE model at 32nm feature size, indicate the superiority of the proposed dual-VDD parallel multiplier utilizing the proposed SSLC in terms of power and power-delay product (PDP) as compared to the single supply multiplier. It is worth mentioning that the proposed low-power multiplier improves static power, average power and PDP by almost 41 %, 42% and 33%, respectively, while maintaining almost the same throughput as compared to the single-supply multiplier.

Keywords: *Low-Power design, Dual-V_{DD}, CNTFET, Voltage level converter, Multiplier, Parallelized.*

1. INTRODUCTION

Maintaining electrostatic integrity in Nano-devices has become a significant task in the recent years. By the continuous scaling of the CMOS technology, many challenges such as intensified short-channel effects, exponentially increased leakage currents and high power density restrict its usefulness for the near future high-density and energy efficient applications. Nowadays, power saving is becoming very significant in arithmetic logic unit (ALU) and memories and especially in the portable battery-powered systems [1, 2]. The equivalent circuit carbon nanotube field effect transistor (CNTFET) is considered as a promising alternative device for the bulk silicon MOSFET due to its superior electrical properties such as significantly high I_{ON}/I_{OFF} and subthreshold swing and also the computed quantum capacitances from the charge in the channel [3,4,5]. In the Model of model CNT quantum inductance, assumed constant and equal to 4 pH/nm, which have splitted up into two inductances of 2 pH/nm, while the classical self-inductance can be ignored.

The threshold voltage (Vt) of a CNTFET is determined according to the diameters of its nanotubes as given in Eq. (1) [6]. Therefore, multi-threshold design can be accomplished by employing CNTs with different diameters [6, 7, 8].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aE_\pi}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}} \quad (1)$$

where, Eg is the CNT bandgap, e is the unit electron charge, a (≈0.246 nm) is the CNT lattice constant, Eπ (≈3.033ev) is the carbon π- π band energy in the tight bonding model and DCNT is the diameter of nanotubes in nanometer which can be calculated based on the chirality of CNTs (n1, n2) according to Eq. (2) and Eq. (3) [6].

$$D_{CNT} = \frac{\sqrt{3}a_0\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \quad (2)$$

$$D_{CNT} \approx 0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2} \quad (3)$$

CNTFET semi empirical model, based on analytical approximations derived from quantum mechanical simulations of the devices which is based on the hypothesis of fully ballistic transport in a mesoscopic system between two nonreflective contacts. In addition, two coefficients, depending on the subbands minima, have been introduced to evaluate the charge in the channel [5].

In the CNTFET model of [9] due to lighter ensuring compile and shorter execution time, without losing in accuracy, significant improvements have utilized to obtain an easy implementation in simulation.

Low-power design techniques are considered in various levels of abstract-tion, including system, architecture, logic, circuit and devices levels [10, 11, 12, 13, 14,15]. Considering different low-power design techniques, supply voltage scaling is an effective approach for reducing static and dynamic power dissipations and consequently, low-power and robust circuits design techniques have become very crucial in the nanoscale era. The total power consumption of a digital CMOS circuit can be calculated according to Eq. (4) and Eq. (5) as described in detail in [13].

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{static} \quad (4)$$

$$P_{total} = V_{DD} \cdot f_{clk} \cdot \sum_i \left(V_{swing,i} \cdot C_i \cdot \alpha_i\right) + V_{DD} \cdot \sum_i I_{sc,i} + V_{DD} \cdot \sum_i I_{l,i} \quad (5)$$

It can be inferred from Eq. (5) that reducing the supply voltage has a considerable impact on all of the power consumption components. However, due to speed constraints, the supply voltage of the blocks located on the critical paths cannot be scaled to the values lower than a specific value. As a result, for low-power design under a specific performance constraint, multi-V_{DD} for different voltage regions is an attractive methodology. In these designs, the signals from the high-V_{DD} (V_{DDH}) region can enter the low-V_{DD} (V_{DDL}) region with no problem. However, the signals of the V_{DDL} region should be passed to the V_{DDH} region through voltage level converters (LCs), which results in power, delay and area redundancies. As a result, minimizing the cost of the level conversion step is a significant issue in multi-V_{DD} designs. Generally, single-supply LCs (SSLC) are more of interest in comparison with the dual-supply voltage level converters (DSLCs) according to their less complexity, lower overall system cost and less crowding in supply-voltage routing [16].

In this paper, a robust and energy efficient SSLC based on CNTFETs is proposed, which outperforms the existing level converters in terms of performance and energy efficiency. In addition, in order to demonstrate the effectiveness of the proposed SSLC in low power design, a CNTFET-based low-power multiplier using parallelism and dual supply voltages is suggested. The simulation results indicate the considerably lower power consumption and PDP of the suggested multiplier as compared to its single supply counterpart.

The rest of the paper is organized as follows: In Section 2, the related level converters are briefly reviewed. Section 3, the proposed SSLC and dual-V_{DD} multiplier are described. Section 4 contains the simulation results, comparisons and discussions. Finally,

Section V concludes the paper.

2. A BRIEF REVIEW OF THE LEVEL CONVERTERS

Different low-voltage and low-power circuits with different design styles have been presented in the literature. The SSLC suggested in [17] (SSLC1), utilizes a diode-connected nMOS transistor in its pull-up network for low voltage converting. In this design, the input signal is connected to both NMOS and PMOS transistors. Hence, for ultra-low-voltage (ULV) input signals, where the input signal is logic ‘1’, both input nMOS and pMOS transistors turn ON which leads to a considerably high static power dissipation. The SSLC of [18], (SSLC2) uses the stacking technique in its both input and output stages, which reduces the power consumption and PDP but increases the delay and design complexity. The SSLC presented in [16] (SSLC3), utilizes dynamically body biased input transistor and diode-connected nMOS transistors in the pull-up network to increase the strength of the input nMOS transistors for up-converting ULV input signals. Moreover, a second-stage circuit is added to provide a full-swing output. Accordingly, the number of the transistors is increased and the speed of the circuits is degraded. The design of (DSLC) in [19] employs dual supply voltages. In this LC, when the input signal is at logic ‘0’, the transistors in the pull-up path turned ON and the drain node of the input transistor is charged. However, the voltage of this node is lower than V_{DDH}. This is due to the fact that, when the voltage at this node crosses the switching threshold voltage of the output inverter, the output voltage commences to discharge. Accordingly, before the voltage of the drain node of the input transistor reaches to V_{DDH}, the output voltage decreases to zero. As a result, the nMOS transistor, which its gate is connected to the output node, turns OFF and subsequently the current mirror cuts OFF. Therefore, the drain node of the input transistor is not continuously charged V_{DDH}. This incomplete voltage lower than V_{DDH} is not able to turn OFF the pMOS transistor of the output inverter completely. As a result, static power dissipation increases and this situation becomes worse in nanoscale technologies.

In the CNTFEET-based level converter presented in [5], (SSLC4), the Vt of the CNTFETs are determined by adopting specified diameters for the CNTs. In order to convert ULV input signals, DCNT/Vt of the CNTFETs are adopted as 2.2nm/0.2V, 0.55nm/0.8V and 1.5nm/0.3V.

Another SSLC5 of [20] utilizes diode-connected nMOS in the pull-up network and low-Vt input nMOS transistors to convert low voltage input signals. Also, source biasing in this design reduces leakage power.

3. PROPOSED WORK

The proposed CNTFET based SSLC is shown in Figure 1. The proposed SSLC is composed of two modified inverters. The first inverter with low voltage input signal consists of a p-type CNTFET (M3) with DCNT/Vt of 0.65nm/0.7V and two stacked n-type CNTFETs (M1 and M2) with DCNT/Vt of 1.5nm/0.3V. The second inverter is a normal inverter (M4 and M5) with DCNT/Vt of 1.5nm/0.3V, which generates the full-voltage swing at the output.

In order to convert an ultra-low-voltage input signal to V_{DDH} at the output, the strength of M1 and M2 must overcome M3. Hence, according to the voltage level conversion, a higher Vt is adopted for M3. For converting a 0.3V input voltage to a 1V output, according to the difference between V_{DDH} and V_{in} (V_{DDH} - V_{in} =0.7V) the Vt of M1 and M2 is adopted as 0.3V and the Vt of M3 is adopted as 0.7V.

Due to the considerable DIBL effect when V_{GS}=0V but V_{DS}=V_{DD} [20], the

OFF state leakage current reduction is a significant issue in nanoscale circuits. In the proposed SSLC, by connecting the input signal to the source node of the M4 transistor a lower V_{DS} (V_{DDH} $-V_{in}$ instead of V_{DDH}) is achieved. When the input signal is '1', the first inverter complements the input signal and subsequently, the input signal of the second inverter becomes 0V. Therefore, M4 turns OFF, M5 turns ON and Vout reaches V_{DDH}. In this situation, the V_{DS} of the OFF transistor M4 is reduced to V_{DDH} $-V_{DDL}$ and the leakage current is considerably reduced. When the input signal is '0, V_{in} provides a ground for the second stage inverter and V_{Out} becomes 0V. In addition, stacking of the M1 and M2 transistors leads to a large reduction in the static OFF current. The stacked devices between supply and ground nodes increase the resistance of this path. Moreover, the V_{DS} of the transistors are reduced which leads to lower DIBL effect and consequently lower OFF current. Furthermore, the threshold voltage of M2 increases due to its higher V_{BS}, which leads to lower leakage current [21, 22]. As a result, the static power of the proposed design decreases.

The proposed SSLC can be utilized effectively in the structure of VLSI circuits. Multiplier is one of the most important arithmetic units and is usually located on the critical path of in digital signal processing and microprocessors.

The structure of a dual-V_{DD} 4-bit multiplier [20] using the proposed SSLC is shown in Figure 2. In this design, the input signals with the voltage swing of V_{DDH} enters the AND unit which generates the partial products with V_{DDL} swing. However, only one of the AND gates, which directly computes M0, utilizes V_{DDH}. The subsequent half adder (HA) and full adder (FA) units with V_{DDL} reduce these partial products and also produce the M1 output, as shown in Figure 2. Finally, a carry ripple adder and an XOR gate compute the remained outputs (M3 to M7).

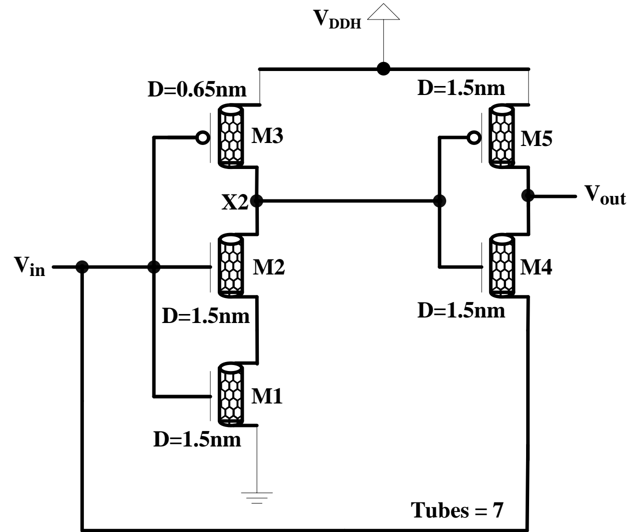


***Figure 1**. The schematic of the proposed SSLC.*

The transistor level structures of the utilized HA and FA circuits have been presented in detail in [23, 24].

As the voltage swing of the output signals of the multiplier is V_{DDL}, the proposed SSLCs are inserted to shift the level of these signals to V_{DDH} to provide a low-power communication with other V_{DDH} blocks. The abovementioned dual-V_{DD} multiplier is more suitable for specific applications where power is significantly more important than performance [20]. In this design, the operation frequency is reduced due to the voltage reduction. For instance, with a 0.65V VDDL and a 1V V_{DDH}, the operating frequency is almost halved as compared to the multiplier with a single supply of 1V. While the dynamic and static power consumptions and PDP are reduced, the throughput is also halved.

Hence, according to the parallelism method [25], a dual-V_{DD} parallel multiplier is designed to compensate this frequency and throughput degradation.

The block diagram of the reference single-V_{DD} multiplier and the parallelized dual-V_{DD} multiplier are shown in Figure 3.

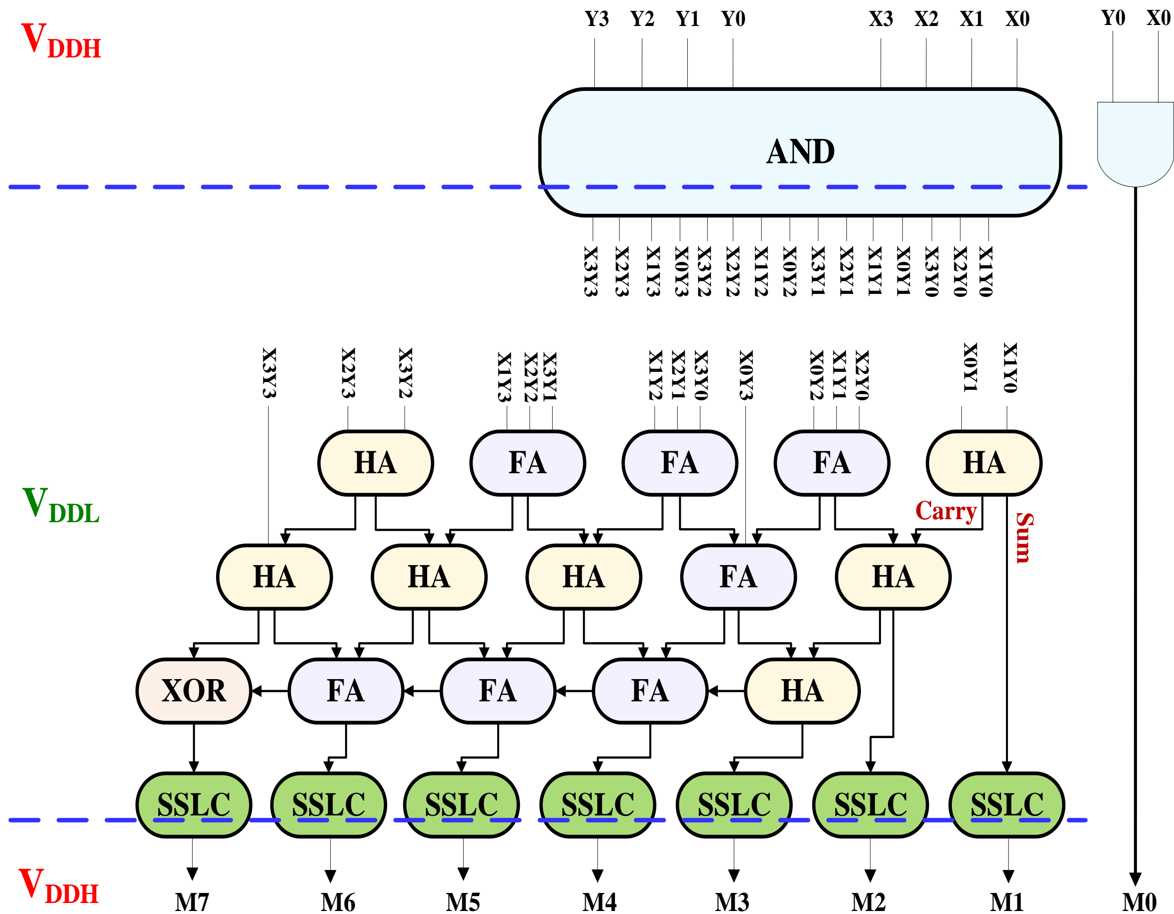


Figure 2. The block diagram of the dual-V_{DD} low-power multiplier using the proposed SSLC.

As shown in Figure 3 (b), two identical multipliers are used. In addition, the upper input registers are sensitive to the rising edge of the clock pulse and the other input registers are sensitive to the falling edge of the clock pulse. This allows each multiplier to operate at half the original frequency while maintaining the original throughput. Since the speed requirement for this parallelized circuit has been almost halved, the supply voltage can be dropped to the voltage at which the delay is almost doubled. While the capacitance increases by a factor of about two, the operating frequency is reduced by a factor of almost two as well. As reducing the supply voltage has a quadratic impact on the dynamic power consumption, the dynamic power consumption is significantly reduced, while the original throughput is maintained. However, the overheads of the multiplexers and specifically the required voltage level converters should be considered.

The significant power reduction in the parallelism method for low-power designs is provided with a cost of highly increased transistor count. It is worth mentioning that the reduced voltage swing in a considerable part of the circuit will considerably alleviate the aging effects, as one of the most important issues in the recent technologies and increases the effective lifetime of the integrated circuits [26].

4. SIMULATION RESULTS AND COMPARISONS

In this section, the performance metrics and effectiveness of the proposed SSLC are evaluated and compared with the other existing level converters.

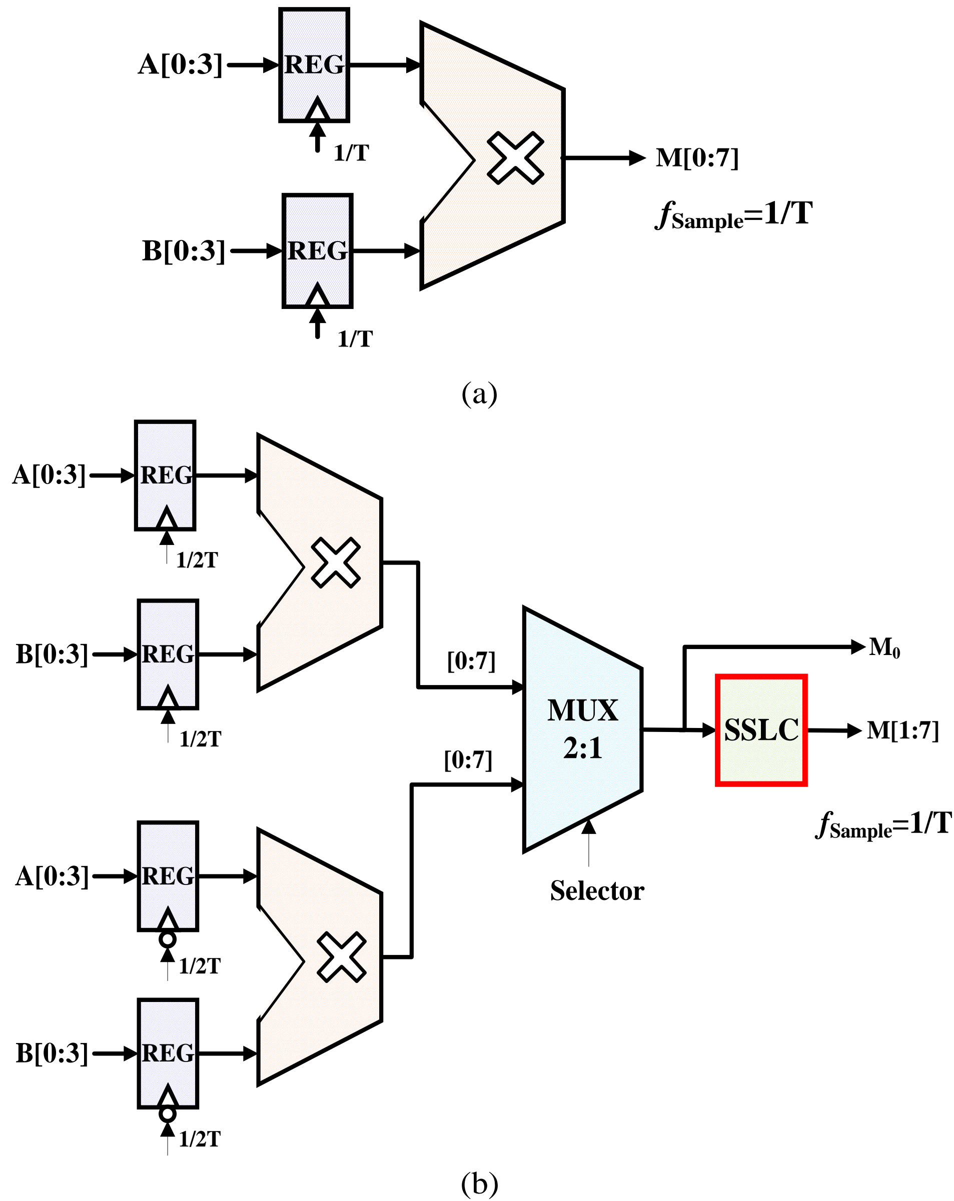


Figure 3. The block diagram of the multiplier: a) single supply design, b) Dual-V_{DD} parallelized design using the proposed SSLC.

In order to have fair comparisons, each design is optimized in terms of energy efficiency and leakage currents with consideration of presented CNTFET model of [3, 4, 5]. Therefore, results are simulated using the valid Stanford CNTFET HSPICE model at 32nm technology node. Some of the important parameters of the CNTFET model are listed in Table 1.

The simulation results of the level converters, considering V_{DDH}=1V, f=8GHz and CL=0.5 fF, are given in Table 2. The results demonstrate the superiority of the proposed level converter especially in terms of power consumptions and energy efficiency. Utilizing the stacking technique in all paths in SSLC2 results in power reduction with the expense of a considerable speed degradation.

Furthermore, as SSLC2 doesn't work at input signals with voltage swing lower than 0.6V, it is not considered as a low-voltage design. As stated before, in DSLC [19] when the input signal is at logic '0', the incomplete voltage at the input node of the output inverter turns

ON the nMOS transistor of the output inverter, but it is not able to turn OFF its pMOS transistor and consequently power dissipation increases.

Although the SSLC4 of [8] has less power consumption as compared to the all designs of [16, 17, 18, 19, 20], but has highest delay compared to the designs of [17, 18, 19, 20]. However, in the proposed SSLC, by utilizing dual-chirality CNTFETs, source biasing and decreasing the DIBL effect, the power consumption and PDP are considerably reduced.

Systematic and random process variations and noise are among the most significant challenges ahead of designing nanoscale circuits, which can negatively affect their robustness and energy-efficiency [27]. Experimental results show that the mainly variations in CNTFET-based circuits are variations in the CNT density which occurs due to the variations in the spacing between CNTs and CNT count [28]. In addition, the impact of CNT diameter variation become more important in multi-diameter CNTFET-based circuits.

In order to evaluate the process variations effect, Monte Carlo simulations have been conducted by modeling the CNT diameter and density with ±5% to ±15% Gaussian distributions and variation at ± 3σ level.

The performance parameters of the designs in the presence of major CNTFET process variations are shown in Figure 4 and figure 5. The results demonstrate the correct operation of the proposed SSLC with smaller parametric variations even in the presence of process variations, as compared to the other optimized CNTFET-based designs.

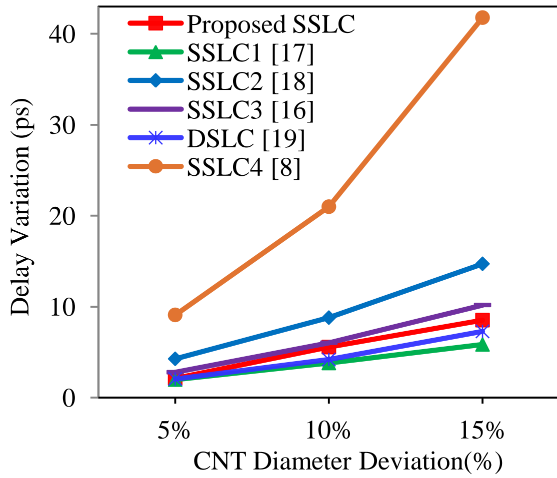
Also, in order to evaluate the effectiveness of the proposed efficient level converter, the single-supply and the suggested dual-supply multipliers, described in the previous section, are considered for simulation.

Table 1. *The CNTFET parameters.*

Parameter	Value
Physical channel length	32 nm
The mean free path in the intrinsic CNT	100 nm
The length of doped CNT drain-side region	32 nm
The length of doped CNT source-side region	32 nm
The mean free path in p^+/n^+ doped CNT	15 nm
The distance between the centers of two adjacent CNTs within the same gate	≤30 nm
Sub-lithographic pitch	4 nm
The thickness of high-k top gate dielectric	4 nm
The dielectric constant of high-k top gate dielectric material (HfO_2)	16
The dielectric constant of substrate (SiO_2)	4
The coupling capacitance between the channel region and the substrate (SiO_2)	40 aF/m
The Fermi level of the doped S/D CNT	6 Ev
The work function of S/D metal contacts	4.6 eV
CNT work function	4.5 eV

Table 2. *Simulation results of the LCs (V_{DDH}=1V and f=8 GHz)*

Level Converter	V_{in} (V)	Delay (ps)	Average Power (uW)	PDP (aJ)	Static power (nW)
Proposed SSLC	**0.4**	**10.05**	**4.62**	**46.53**	**8.54**
	0.5	**9.65**	**4.77**	**46.10**	**0.53**
	0.65	**9.45**	**5.03**	**47.59**	**0.20**
SSLC1 [17]	0.4	10.93	9.65	105.65	280.8
	0.5	10.49	7.62	79.964	73.21
	0.65	9.05	7.04	63.823	12.4
SSLC2 [18]	0.4	Don't work			
	0.5				
	0.65	16.42	8.25	135.65	4.5
SSLC3 [16]	0.4	20.10	13.26	266.69	260
	0.5	19.84	12.86	255.31	52.5
	0.65	19.46	12.43	252.35	4.67
DSLC [19]	0.4	26.52	12.1	321.00	1.61
	0.5	15.90	11.59	184.31	1.64
	0.65	9.95	11.93	118.79	1.68
SSLC4 [8]	0.4	18.73	6.54	122.6	2.36
	0.5	18.22	6.52	118.96	2.20
	0.65	18.11	6.5350	118.37	2.19
SSLC5 [20]	0.4	11.93	7.65	91.28	261.3
	0.5	9.35	6.58	61.6	54
	0.65	9.63	6.1	59	6.18



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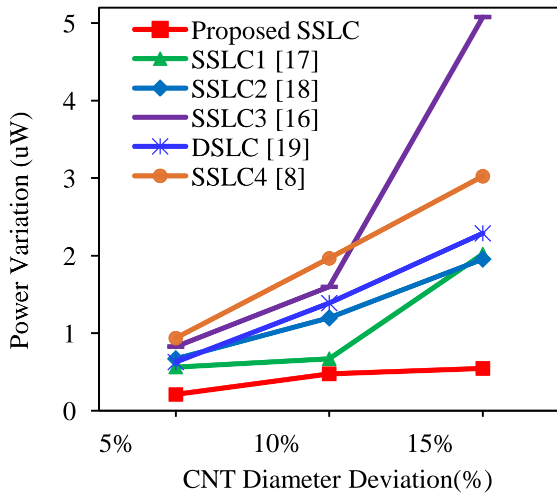

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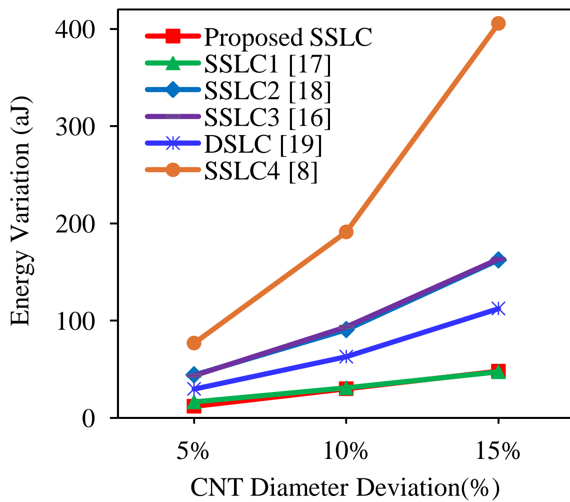
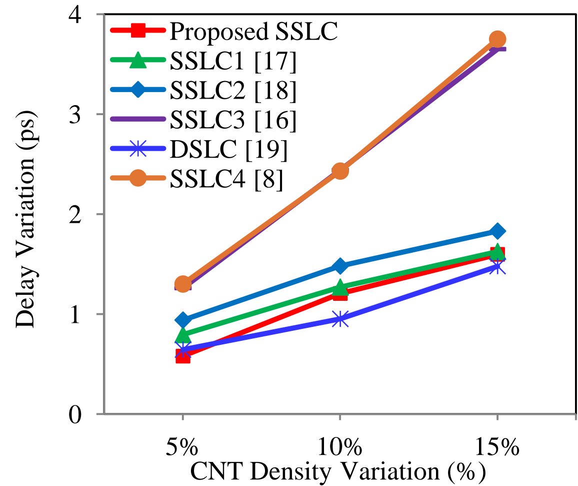


(c)

Figure 4. *Simulation results at the presence of CNT diameter variations.*



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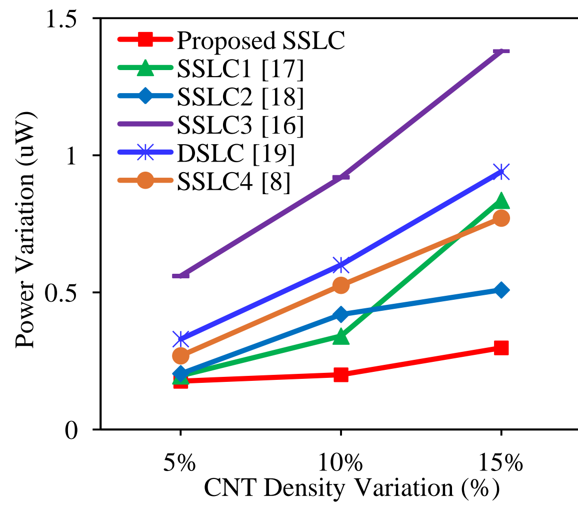

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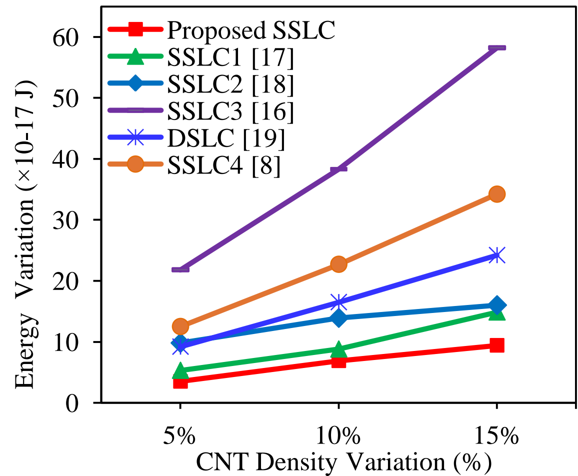

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Figure 5. *Simulation results at the presence of CNT Density variations.*

Indeed, the 4-bit multiplier as a benchmark with a high supply voltage (1V) without level converter and the 4-bit parallelized multiplier with dual-V_{DD} of 1V as V_{DDH} and 0.65V as V_{DDL} using the proposed SSLC are compared in Table 3. According to the results, the proposed design leads to lower average power consumption, static power dissipation and PDP, while maintaining a comparable performance as compared to the single supply multiplier.

Table 3. *Simulation results of the multipliers ($f_{Sampling}$=8GHz)*

Multiplier Circuit	Delay (ps)	Average Power (uW)	PDP (× 10-15J)	Static power (uW)
Multiplier Without LC V_{DD}=1V	49.55	220.74	11	5.64
Parallel Multiplier V_{DDH} = 1V, V_{DDL} = 0.65V	**50.12**	**129.53**	**6.5**	**3.70**

5. CONCLUSION

In this paper, an efficient Single Supply Level Converter and a dual-V_{DD} parallel multiplier for low power and high-performance applications have been proposed. In a multi-V_{DD} system, voltage islands to communicate with each other, low power, and low-cost LC is required. In the proposed SSLC, dynamically-controlled source voltage decreased drain induced barrier lowering (DIBL) effect, suitable CNT diameter to provide Multi-Vt transistors have been utilized properly in order to reduce the power consumption without performance degradation. The proposed SSLC has been utilized in the proposed dual-V_{DD} parallel multiplier. Each design has been optimized based on mentioned CNTFET Models and simulated using the HSPICE Stanford CNTFET model at 32nm. The simulation results demonstrate the superiority of the proposed designs, especially in terms of average and static powers delay and PDP. The proposed dual-V_{DD} parallel multiplier with proposed SSLC as compared to the single supply multiplier without LC was about on average 42 %, 41%, and 33% lower total average power, static power and PDP respectively.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. Moaiyeri, M. H., Akbari, H., Moghaddam. M, "An ultra-low-power and robust ternary static random access memory cell based on carbon nanotube FETs", *Journal of Nanoelectronics and Optoelectronics*, 13 (2018) 617-627.
2. MoghaddamMoghaddam, M., Timarchi, S., Moaiyeri, M. H., Eshghi, M., "An Ultra-Low Power 9T SRAM Based on Dynamic Threshold Voltage Techniques", *Circuits, Systems, and Signal Processing*, 35 (2016) 1437-1455.
3. Marani, R., Perri, A. G., "A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors Oriented to Simulation Software*", Current Nanoscience*, 7 (2011) 245-253.
4. Marani, R., Perri, A. G., "Static Simulation of CNTFET-based Digital Circuits", *Int. J. Nanosci. Nanotechnol*., 14 (2018) 121-131.
5. Gelao, G., Marani, R., Perri, A. G., "A Semiempirical SPICE Model for n-Type Conventional CNTFETs", *IEEE Transactions on Nanotechnology*, 10 (2011) 506-512.
6. Liang, J., Chen, L., Han, J., and Lombardi, F., "Design and Evaluation of Multiple Valued Logic Gates Using Pseudo N-Type Carbon Nanotube FETs*", IEEE Transaction on Nanotechnology*, 13 (2014) 695-708.
7. Rezaeikhezeli M., Moaiyeri, M. H., Jalali, A., "Analysis of Crosstalk Effects for Multiwalled Carbon Nanotube Bundle Interconnects in Ternary Logic and Comparison with Cu interconnects", *IEEE Transactions on Nanotechnology*, 16 (2017) 107 – 117.
8. Moghaddam, M., Moaiyeri, M. H., Eshghi, M. Jalali, A., "*Low-voltage multi-VTH single-supply level converters based on CNTFETs*", The 22nd Iranian Conference on Electrical Engineering, Tehran, Iran, (2014) 366-370.

9. Marani, R., Perri, A. G., "Dynamic Simulation of CNTFET-Based Digital Circuits", *Int. J. Nanosci. Nanotechnol.*, 14 (2018) 277-288.
10. Hinds, M., Sparkman, B., Di, J. and Smith, S., "An Asynchronous Advanced Encryption Standard Core Design for Energy Efficiency", *Journal of Low Power Electronics*, 9 (2013) 175-188.
11. Zarhoun, R., Moaiyeri, M. H., Shirinabadi Farahani, S., Navi, K., "An Efficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotube FETs", *Electronics and Telecommunications Research Institute (ETRI) Journal*, 36 (2014) 89-98.
12. Moghaddam, M., Moaiyeri, M. H., Eshghi, M., "Design and Evaluation of an Efficient Schmitt Trigger-based Hardened Latch in CNTFET Technology," *IEEE Transactions on Device and Materials Reliability (TDMR)*, 17 (2017) 267-277.
13. Rabaey, J. M., "*Low power design essentials*," Springer Science & Business Media (2009).
14. Marani, R., Perri, A. G., "A Procedure to Analyze a CNTFET-Based NOT Gate with Parasitic Elements of Interconnection Lines", *Int. J. Nanosci. Nanotechnol*, 17 (2021) 161-171.
15. Sayyah Ensan, S., Moaiyeri, M. H., Moghaddam, Hessabi, Sh., "A low-power single-ended SRAM in FinFET technology," *International Journal of Electronics and Communications (AEÜ),* 99 (2019) 361-368.
16. Moghaddam, M., Eshghi, M., Moaiyeri, M. H., "A Low-Voltage Single-Supply Level Converter for Sub-VTH /Super-VTH Operation: 0.3V to 1.2V", *International Journal of Computer Applications*, 69 (2013) 14-18.
17. Puri, R., Stok, L., Cohn, J., Kung, D. S., Pan, D. Z., Sylvester, Srivastava, D., Kulkarni, S., "Pushing ASIC Performance in a Power Envelope", *Proceedings of 40th ACM/IEEE Design Automation conference*, (2003) 788-793.
18. Kumar, M., Arya, S. K., Pandey, S., "Level Shifter Design for Low Power Applications", *International journal of computer science & information Technology*, 2 (2010) 124-132.
19. Hosseini, S. R., Saberi, M., Lotfi, R., "A Low-Power Sub-threshold to Above-Threshold Voltage Level Shifter", *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61 (2014) 753-757.
20. Moghaddam, M., Moaiyeri, M. H., Eshghi, M., Jalali, A., "A Low-Power Multiplier Using an Efficient Single-Supply Voltage Level Converter", *Journal of Circuits & Systems and Computers*, 24 (2015) 1550124-1 - 1550124-15.
21. Roy, K., Mukhopadhyay, S., Mahmoodi-Meimand, H., "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits*", Proceedings of the IEEE,* 91 (2003) 305-307.
22. Moghaddam, M., Moaiyeri, M. H., Eshghi, M., "FinFET Based Level Converter for Multi-VDD System Design", *CSI Journal on Computer Science and Engineering (JCSE),* 14 (2017) 23 - 28.
23. Zimmerman, R., Fichtner, W., "Low-Power Logic Styles: CMOS versus pass-transistor logic", *IEEE Journal on Solid-State Circuits*, 32 (1997) 1-12.
24. Goel S., Kumar, A., Bayoumi, M. A., "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style", *IEEE Transactions on Very Large Scale Integration*, 14 (2006) 1309–1321.
25. Chandrakasan. A. P., Sheng, S., Brodersen, R.W., "Low-power CMOS digital design", *IEICE Transactions on Electronics*, 75 (1992) 371-382.
26. Kaul, H., Anders, M., Hsu, S., Agarwal, A., Krishnamurthy, R., Borkar, Sh., "Near-threshold voltage (NTV) design: opportunities and challenges", *Proceedings of the 49th Annual Design Automation Conference*, (2012) 1153-1158.
27. Marani, R., Perri, A.G., "Comparative Analysis of Noise in Current Mirror Circuits based on CNTFET and MOS Devices", *Int. J. Nanosci. Nanotechnol*., 17 (2021) 123-131.
28. Zhang, J., Patil, N., Wong, H.-S. Ph., Mitra S., "Overcoming Carbon Nanotube Variations through Co-optimized Technology and Circuit Design", *IEEE International Conference on Electron Devices Meeting (IEDM)*, (2011) 4.6.1-4.6.4