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Analysis of Temperature Effects in the Design of CNTFET-based Analog Circuits

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Abstract

In this paper we analyzed at first the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance, the transconductance. Then, using ADS software, the effects of temperature variations in the design of some analogue circuits, such as a harmonic oscillator and an operational transconductance amplifier (OTA), are illustrated and widely discussed.

Keywords: *CNTFET, Modelling, Temperature effects, I-V characteristics, Harmonic oscillator, OTA.*

1. INRODUCTION

Carbon NanoTubes, also known with the acronym CNTs (Carbon NanoTubes), have unique electronic and mechanical properties that make them promising candidates for future nanotechnology applications [1]. In particular CNTs, for their extraordinary electronic properties, are used as channel in CNTFETs (Carbon Nanotube Field Effect Transistors), contrary to MOSFETs devices, where the channel is of silicon.

For conventional CNTFET, we already proposed a compact, semi-empirical model [2]. Then we introduced some improvements [3-6] to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A, and our model has been implemented to carry out analysis of CNTFET-based A/D circuits [7-11].

In this paper we analyzed at first the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance and the transconductance.

Then, starting from these characteristics, we studied the effects of temperature variations in the design of a harmonic oscillator and an Operational Trans-conductance Amplifier (OTA).

The obtained results are illustrated and widely discussed, emphasizing that the proposed procedure can easily be applied to any other circuit based on CNTFET.

The presentation is organized as follows.

A brief review of CNTFET model is presented in Section 2, while Section 3 describes the temperature variations on I-V characteristics, on transconductance and on output resistance of the CNTFET considered. The design of a harmonic oscillator and of an OTA are described in Sections 4 and 5, together with the discussion of simulation results. The conclusions and future developments are described in Section 6.

2. A BRIEF REVIEW OF OUR CNTFET MODEL

2.a I-V model

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them. In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [12], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT}, have the expressions reported in [2-3].

2.b C-V model

An exhaustive description of our C-V model is widely described in our References [9-11] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD}=q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS}=q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behavior, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances. We have achieved this goal using an empirical method exhaustively described in [2-3]. In this way all elements of the equivalent circuit of Figure 1 can be determined.

It is similar to a common MOSFET one [13] and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD}, the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

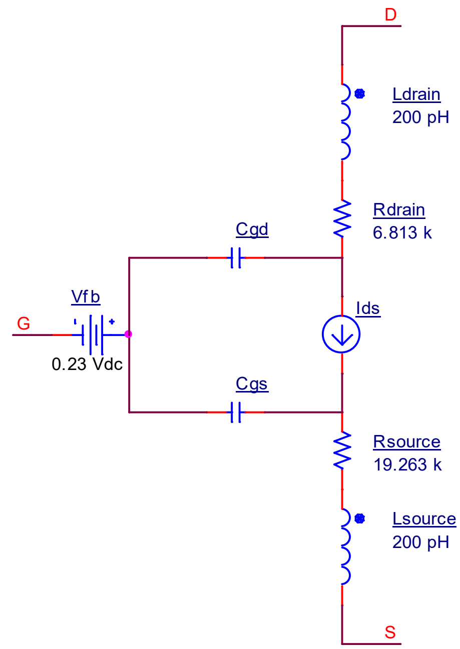

Figure 1. *Equivalent circuit of a n-type CNTFET.*

3. TEMPERATURE EFFECTS ON I-V CHARACTERISTICS

To investigate on the I-V CNTFET characteristics in different temperatures, we consider a single wall n-CNTFETs with a diameter of 1.509 nm and 22 nm long in the ballistic transport hypothesis.

We design a standard simulation circuit where, in static conditions, alternately we were changing V_{GS} and V_{DS} and vice versa.

We performed the analysis at 100 K, 300 K and 500 K as shown in Figure 2 and Figure 3.

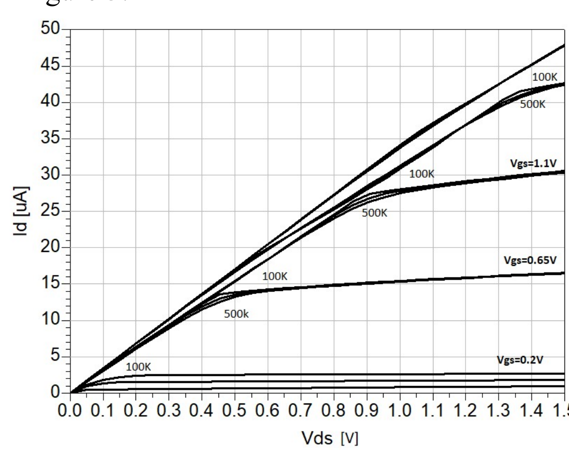

Figure 2. *I_{DS} versus V_{DS}.*

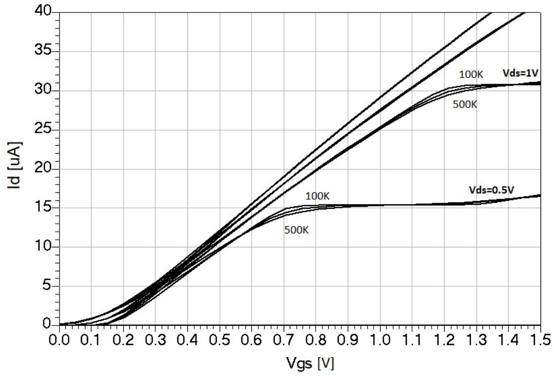

Figure 3. *I_{DS} versus V_{GS}.*

From the analysis of Figures 2 and 3, we can say that the increasing temperature at lower quiescent voltages leads to a lower drain current, especially on the knee of the curve. This is a MOSFET technology common feature that guarantees a negative current feedback that prevents the device break at higher temperatures.

It can easily see that those curves suffer a negligible variation in terms of I_{DS} in the extreme conditions of 100 K and 500 K.

Moreover these changes are often comparable with the CNTFET technological process uncertainties and almost null. The largest variation is in the knee region where we measure an I_{DS} of 13.4 uA at 500 K and I_{DS} of 15.1 uA at 100 K for V_{GS} = 0.7 V and V_{DS} = 0.5 V.

We investigate about the other design parameters of CNTFET, i.e. the transconductance and the output resistance of the device. As you can see hereafter, in these cases we discover larger differences than the previous ones so we decided to extend the analysis to intermediate temperature values (200 K and 400 K).

We adopt a circuit topology able to increase slightly an input voltage and estimate the I_{DS} changes in order to perform differential measurements.

The results of this analysis are reported in the following figures.

In particular in Figure 4 we show the CNTFET transconductance on different working conditions.

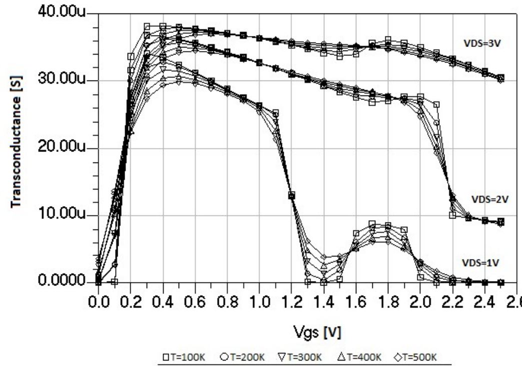

Figure 4. *Transconductance on different temperature conditions.*

A plot of the output resistance, R_{OUT}, fundamental parameter in the design of integrated active loads or mirrors, is reported in Figure 5, whose details (zooms) are shown in Figures 6 and 7.

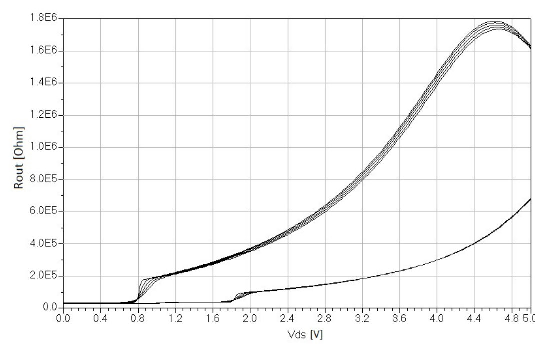

Figure 5. *R_{OUT} versus V_{DS}.*

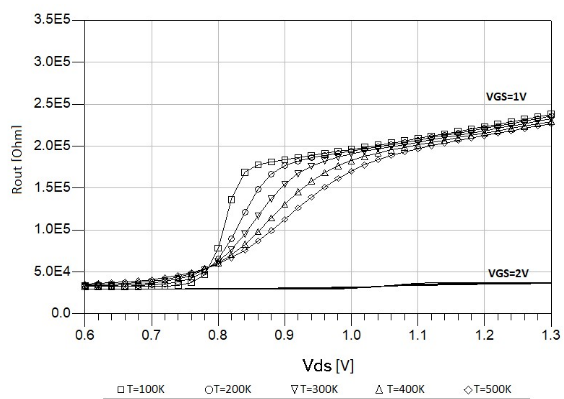

Figure 6. *R_{OUT} versus V_{DS} (zoom),*

The output impedance trend does not change in different temperature conditions.

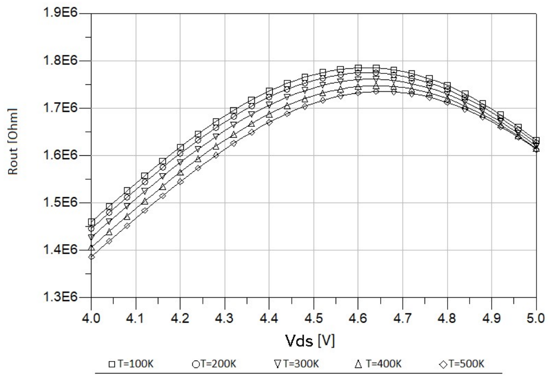

Figure 7. *R_{OUT} versus V_{DS} (zoom).*

It can also easy to recognize the two working regions of the device: the triode region with a very poor output resistance and the saturation region with an impedance next to the MOSFET technology. After the peak at 4.6 V, CNTFET enters in the tunnelling region where I_{DS} increases exponentially and R_{OUT} decreases at the same ratio.

In Figure 6 we find the largest differences after the temperature changes. At lower temperature there is a faster transition that leads to a maximum output resistance larger than in higher temperatures.

4. DESIGN OF A HARMONIC OSCILLATOR

Regarding to the analysis of a harmonic oscillator, in order to analyse the temperature effects, we choose a phase displacement oscillator made of three identical RC cells. We changed the value of each resistor and capacitor to reach a correct working condition with the maximum frequency in a 3.3 V single supply condition.

The circuit used for this simulation is shown in Figure 8.

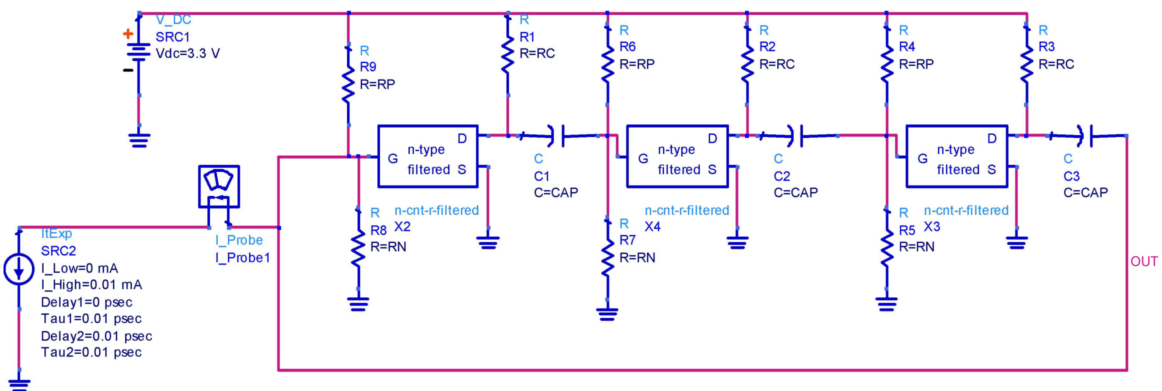

Figure 8. *Harmonic oscillator.*

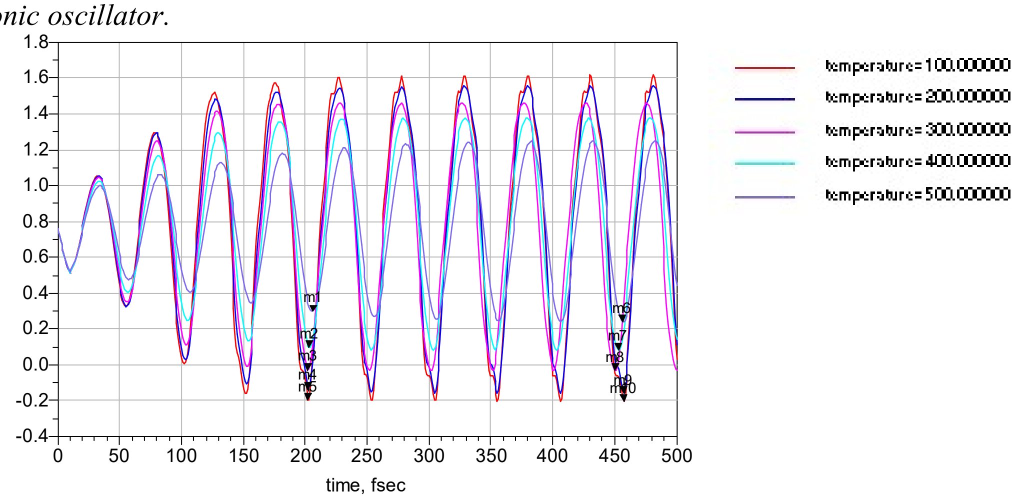

Figure 9. *Harmonic oscillator output.*

To determine the oscillation frequency, we set up a transient analysis. In Figure 9 the output of this device is reported, where the effects of temperature variation can be clearly seen

Decreasing the temperature, we found that the oscillator reached the steady-state condition earlier (according to the higher value of I_{DS}). We could also note that, at lower temperature, the oscillation frequency tends to increase, as shown in Figure 10.

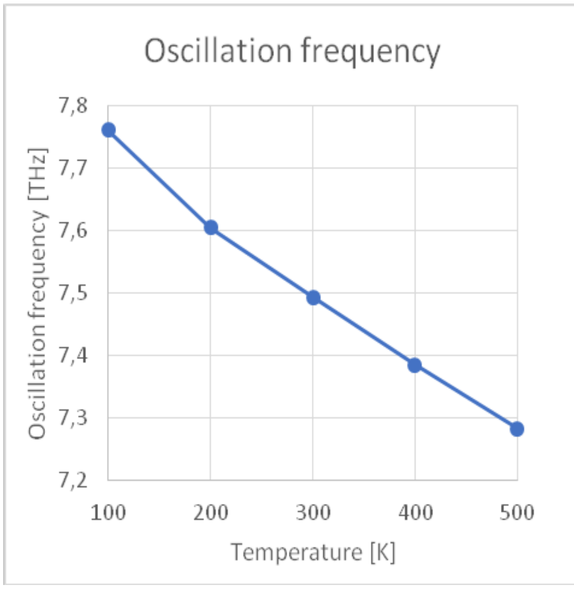

Figure 10. *Oscillation frequency vs temperature.*

Moreover, we measured the temporal distance between minima points of the sinusoid in regime state, choosing a 20-period distance to decrease the time evaluation error.

For the calculations, we estimated a maximum error of 0.1 ps and we noticed that the previous graph uncertainty is much less than the overall trend so we can affirm that the oscillation frequency slope reported is independent from numerical noise. We also noticed that at higher temperature the oscillation amplitude decreases according to the decreasing of I_{DS} (note that the working condition is not in the high voltage region).

During the simulations, we optimized the circuit parameters trying to produce a spurious free sinusoid at 300 K and this led to abnormal working conditions on 100 K where gain is higher.

As these results show, the optimal working conditions of the CNTFET oscillator are at ambient temperature where we can achieve a discrete output amplitude and a good spectral purity. As we lower the temperature the amplitude of the sinusoid increases but we need a following filtering stage to have a spurious free wave.

At 500 K instead, we obtained a very high purity but with a lower amplitude.

We can conclude that, due to the large variation of CNTFET transconductance on V_{DS}, the oscillator correct behaviour became compromised.

5. DESIGN OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

We want to study the effect of temperature in the design of an OTA reported in Figure 11, where the active load is a cascode current sink mirror [14] working at 3 μA.

In particular, the developed OTA runs with 6 W of power and also presents an high gain due to the cascode active load.

The Voltage Transfer Characteristics (VTCs) at different temperatures are reported in Figure 12, where it is easy to see the proposed OTA has not high gain at low temperatures (near 100 K) but can correctly operate at high temperatures.

Moreover Figure 12 shows the input and output dynamic in different environmental conditions.

We have analysed the current splitting on the differential couple confirming them proper working and the result is shown in Figure 13.

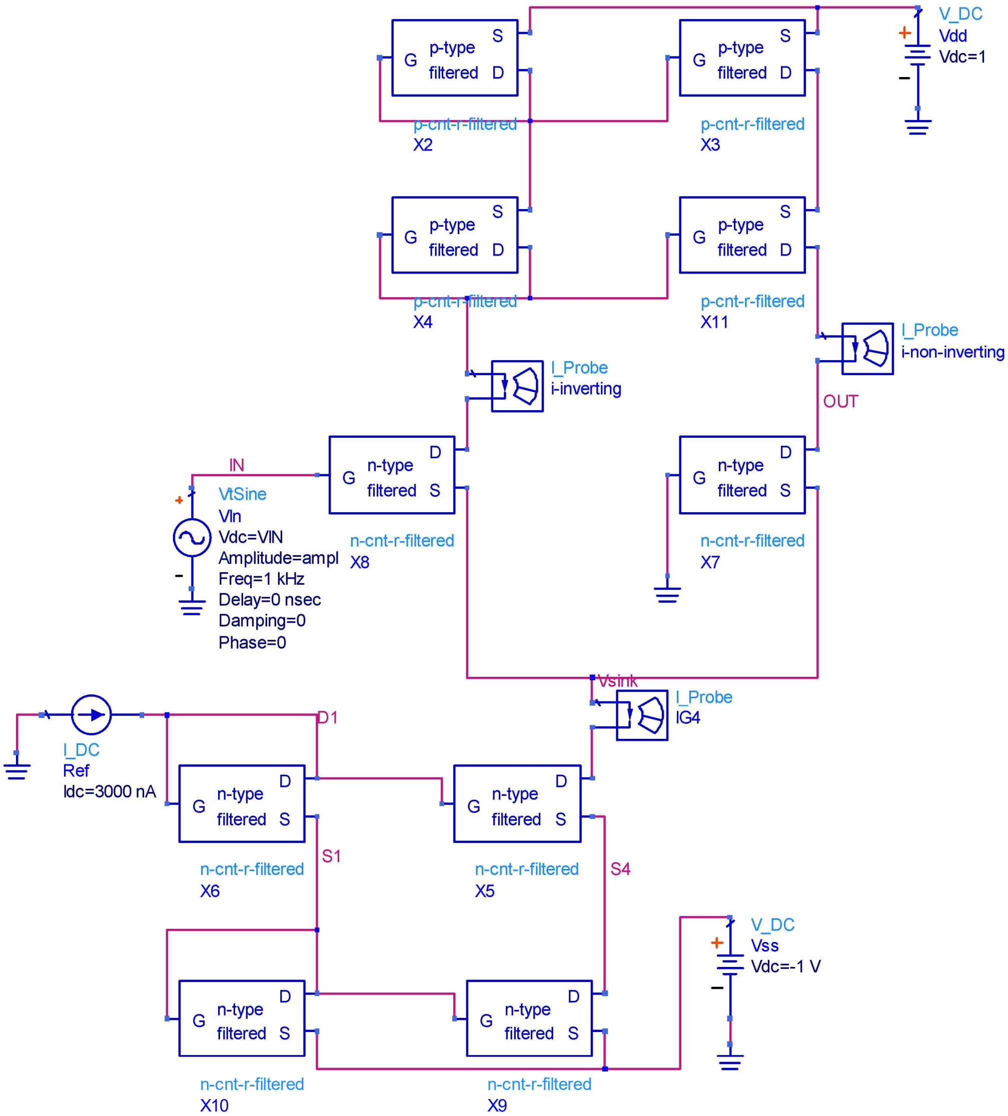

Figure 11. *OTA circuit.*

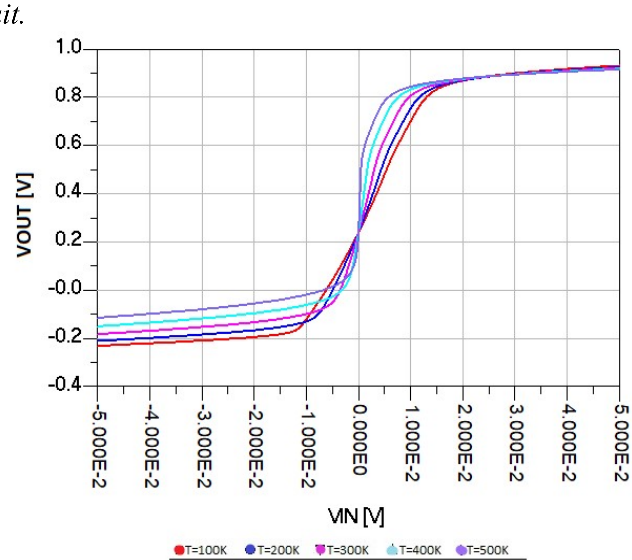

Figure 12. *OTA VTCs vs temperature.*

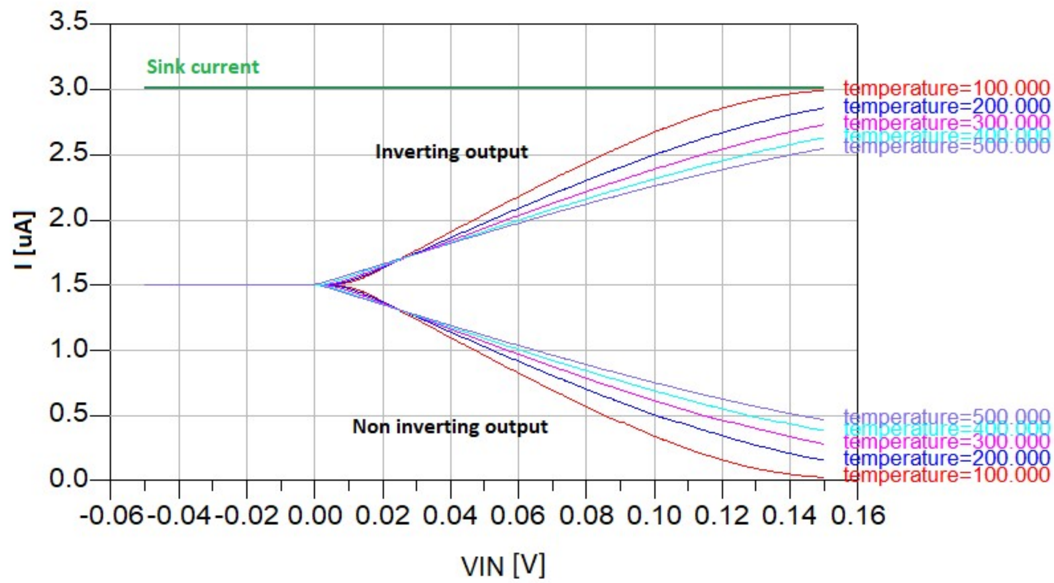

Figure 13. *Differential couple with mirror active load current splitting.*

The total current sinking from the two branches of OTA, labelled "sink" in Figure 13, has no visible dependence neither on input voltage nor on temperature. This is a positive check of the correct working of current mirror.

To determine the differential and common gain, at first we determined the differential gain directly from the VTC curves. Then, we have evaluated the common mode gain from the common mode transfer curves.

This procedure allows to evaluate the Common Mode Rejection Ratio (CMRR) [15], as shown in Figure 14, and amplifier gain, shown in Figure 15 in different temperature conditions.

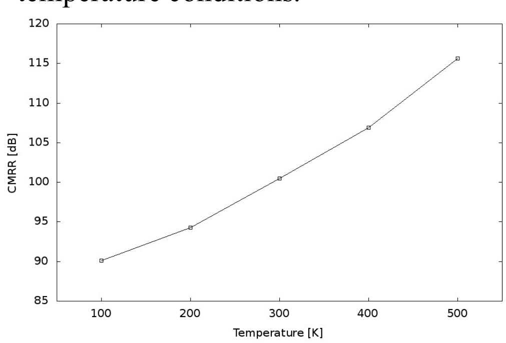

Figure 14. *CMRR versus temperature.*

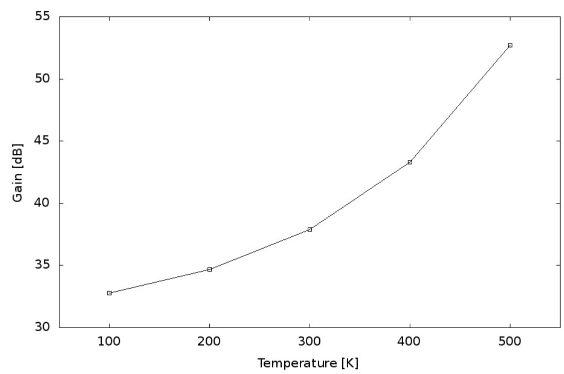

Figure 15. *Amplifier gain vs temperature.*

In the light of the results obtained we can say that our circuit works with high CMRR and moderate gain values, which increase with temperature.

Following the Allen-Holberg procedure [13], it has also been possible to determine the Input Common Mode Range (ICMR) of the proposed OTA at different temperatures.

The results are reported in Figure 16. In particular Figure 16 shows that at T = 100 K the ICMR is (–0.9 V, 0.4 V) and at T = 500 K the ICMR is (–1.0 V, 0.2 V).
Therefore we can affirm that the ICMR changes only slightly.

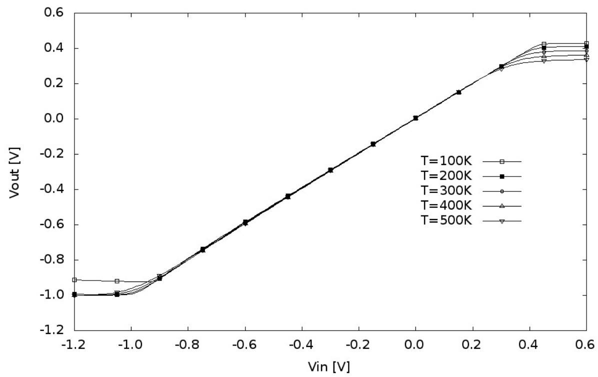

Figure 16. *ICMR versus temperature.*

6. CONCLUSIONS AND FUTURE DEVELOPMENTS

We have analysed at first the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance and the transconductance, using a compact, semi-empirical model, already proposed by us.

To investigate on the I-V CNTFET characteristics in different temperatures, we considered a single wall n-CNTFETs with a diameter of 1.509 nm and 22 nm long in the ballistic transport hypothesis.

From the analysis of CNTFET I-V characteristics, we can affirm that, except for the transition regions, we found very slight differences when temperature changes.

Furthermore, the device behaviour was found to be very MOSFET-like, thus it is possible to adapt the existing circuits to CNTFET ones without difficulties.

Then, using ADS software, the effects of temperature variations in the design of a harmonic oscillator and of an OTA have been illustrated.

In particular the harmonic oscillator circuit manifested a higher dependence on temperature: in fact simulations have shown that the oscillation amplitude increasing causes distortion from 100 K to 200 K.

For the OTA, in which we used a current mirror as an active load, we found a differential gain decreasing at lower temperature. We also noticed a common mode gain decreasing at high temperatures (caused by the mirror higher efficiency) resulting in a considerable CMRR increasing. However, OTA ICMR remains almost the same in all the different conditions, proving that temperature slightly affects CNTFETs performance.

Currently we are studying the effects of temperature [16-17] and of noise [18-21] in other circuits based on CNTFETs and we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [22-23].

Moreover we intend to repeat the proposed design using other CNTFET models such the model proposed in literature [24-27] in order to have comparable results.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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