Int. J. Nanosci. Nanotechnol., Vol. 17, No. 1, March 2021, pp. 11-21

# Design of Encoder Circuit Using Layered NAND and NOR Gates in Quantum Dot Cellular Automata

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*(Received: 30 January 2020 and Accepted: 27 June 2020)*

***Abstract***
*Quantum dot cellular automata or QCA represents a new methodology of quantum computing with the potential for higher performance over existing devices. It adds necessary features such as enhanced speed, smaller size and lower power consumption in comparison to existing CMOS based technology. Based on this study the proposed paper designed three different kinds of encoder circuits using QCA technology. Following paper used layered 2-input NAND gate and NOR gates to design 4 to 2 encoder, priority encoder and octal to binary encoder circuits. The paper also showed the cell count, area, length, breadth & latency calculations for the designed encoder circuits. Proposed circuits are compared with the previously suggested designs in terms of area consumption and cell count. All the circuits designed without majority gate circuit. Potential energy for the designed circuits also calculated to check the stable output and reliability of the circuits.*
***Keywords:*** *Quantum-dot cellular automata, Layered NAND gate, Layered NOR gate, Priority encoder, Latency, Polarization, Octal to binary encoder.*

## 1. INRODUCTION

Current silicon based transistor technology faces serious limitations due to its high power consumption and large feature size, which makes it almost impossible to fit in small scale devices. Nanotechnology proposes a sustainable solution to this problem, which leads to the development of QCA. QCA is used to implement designs with small size, high packing density, and minimum power dissipation [1].

The basic component of a QCA device is the quantum cell. It consists of 4 or 6 quantum dots. One excess electron in the dot causes the polarization of the cell.

Binary information represented in QCA by the position of two mobile electrons in each logic cell. When the barriers between the dots are low enough to free the electrons under the control of the clocking scheme, these two electrons tend to occupy antipodal sites within the cell. This occurs due to the Columbic repulsion in the cell which corresponds to the lowest energy state of the system [2]. Fig.1 shows the polarization of the QCA cell. Let the numbering of the dots (denoted as i ) in the cell goes clockwise starting from the dot on the top right dot i as 1, bottom right dot i as 2, bottom left dot i as 3 and top left dot i as 4.

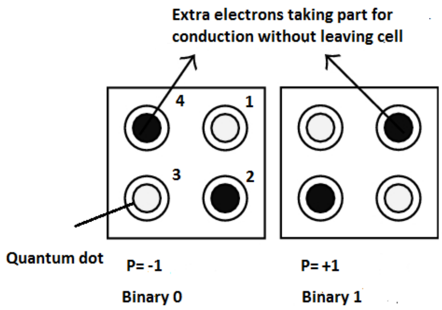



***Figure 1***.*QCA cell polarizations for binary 0 and binary 1.*

Polarization $P$ in a QCA cell is defined as

$$P = \frac{(\rho 1 + \rho 3) - (\rho 2 + \rho 4)}{(\rho 1 + \rho 2 + \rho 3 + \rho 4)} \quad (1)$$

where $\rho_i$ denotes the electronic charge at dot $i$. The polarization measures the charge configuration—that is, the extent to which the electronic charge is distributed among the four dots. Binary information is represented in QCA by using the position of two mobile electrons in each logic cell. The two charge configurations can be used to represent binary "0" and "1" with a polarization of –1 and +1, respectively. The combination of quantum confinement, the Columbic repulsion, and the discrete electronic charge produces bi-stable behavior [3]. Here the electrons are not transferred but the polarization of each cell is transferred. Charge transfer occurs without the movement of electrons from one cell to the other. There are four kinds of QCA structures such as metal dot, semiconductor dot, molecular dot and magnetic dot. Metal dot QCA composed of four aluminum islands (as dots) connected with aluminum oxide tunnel junctions and capacitors. In the metal-island QCA cell, electrons can tunnel between dots via the tunnel junctions. The two pairs of dots are coupled to each other by capacitors. Two mobile electrons in the cell tend to occupy antipodal dots due to electrostatic repulsion [4, 5, 6, 7]. The quantum dots can be made by using semiconductors like Gallium Arsenide (GaAS) and Indium Arsenide (InAs) hetero junction structures with a high-mobility two-dimensional electron [8, 9, 10]. In molecular QCA, each device is built by molecules. The basic concept of molecular QCA is that each molecular QCA cell consists of a pair of identical allyl groups [11, 12]. However, it is still very difficult to fabricate molecular QCA systems with current technologies and no complete circuit using molecular QCA has yet been demonstrated. In the Magnetic Quantum dot Cellular Automata basic cell is a nanoscale nanomagnets, with the sizes between 50nm and 100nm. Magnetic QCA can reach a speed of about 1GHz only which is low when compared to CMOS [13]. However Magnetic QCA has the significant advantage over semiconductor or metal dot QCA that they can operate at room temperature.

In this paper a 4 to 2 encoder circuit, a priority encoder circuit and an octal to binary encoder circuit is designed by QCA technology. The designs are compared with some established designs with respect to cell count, area consumption and latency [14, 15, 16, 17]. Encoder circuits designed in this paper used layered NAND and NOR gates which is discussed in section 2 and compared the design with the previous proposed circuits [18, 19]. Our designed encoder circuits are the first approach using layered NAND gate without using majority gate of QCA. After literature survey for the encoder circuits we have not found sufficient works based on these proposed circuits. In the paper 4 to 2 encoder, 4 to 2 priority encoder and 8 to 3 octal to binary encoder circuits are designed with less number of cells and with valid outputs following the truth table.

Rest of the paper is organized in this way: Section 2 gives the brief idea about QCA devices for the circuit implementation. Section 3 explains the digital design of the encoder circuits using universal gates prior the implementation in QCA technology. Section 4 shows the designs and simulated outputs of the encoder circuits using QCA. Section 5 shows the comparative study with the previous works for the encoder circuits designed in QCA. Section 6 is for the potential energy calculations and section 7 concludes the paper. Lastly section 8 is for the discussion and future scope of the work.

## 2. QCA BASICS

### 2.1. Majority Gate

The basic building block of QCA is a majority gate. It is a 3-input gate with 5 cells, where the output will be high if two or more than two inputs are held high. Therefore, if the inputs are considered to be A, B, C, and output Y, then the logic expression of Y can be written as

$$Y = AB+BC+CA$$

Thus, by fixing the value of one input to the majority gate, either to logic '1' or logic '0',we can design an AND or OR gate, as shown in Fig 2.

M (A, B, 0) = AB [AND Operation]
M (A, B, 1) = A+B [OR Operation]

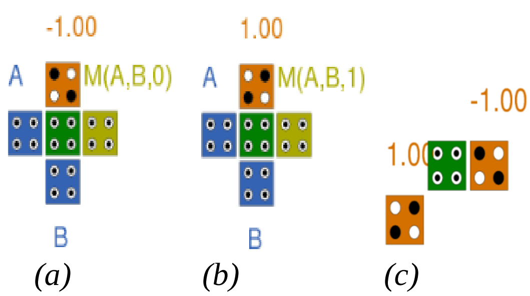



***Figure 2.****(a) The fundamental structure of QCA majority gate as 2- input AND gate (b) 2- input OR gate (c) NOT gate.*

Therefore, using majority gate and NOT gate, any digital logic expression can be realized.

### 2.2. Layered NAND and NOR Gate in QCA

Universal logic Gates such as NAND and NOR Gates which were the first proposed design by the authors in [20] is used to design the encoder circuits. The Universal Gate (UG) design involves the knowledge of new layer, which makes it different from majority voter gate. Unlike Majority voter gate, this gate design has a new layer block in the middle which is set to the polarization of either +1 or -1. Here A, B are the input cells and C the output cell.

The new layer is given polarization +1 to create a NAND gate and -1 to create a NOR gate as shown in Fig. 3.

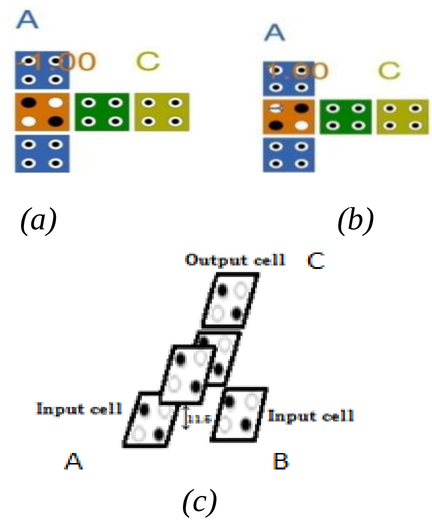



***Figure 3****. (a) NOR gate (b) NAND gate Layered structure.*

Therefore,

NAND Logic = UG (A, B, +1)
NOR Logic = UG (A, B, -1)

## 3. DIGITAL CIRCUITS USING UNIVERSAL GATES

### 3.1. 4 to 2 Encoder Circuit

The digital design of a 4 to 2 Encoder circuit is shown in Fig. 4 whose inputs are decimal digits and outputs are coded representation of inputs. At a time, only one of the input lines is held high and its corresponding binary code is stored in the output pins. Therefore, an N bit encoder consists of 2N input lines and N output lines.

For example, a 4 to 2 encoder has 4 inputs (namely D0, D1, D2 and D3) and 2 output bits (namely Y1, Y0). When D0 is held high, 00 is stored at the output. Similarly, if D2 becomes high, 10 is stored at the output. Table-1 shows the truth table of the Encoder circuit.

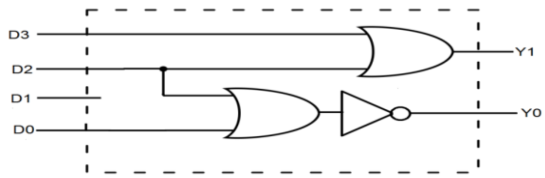



***Figure 4.*** *4 to 2 Encoder circuit diagram.*

***Table 1.*** *Truth table of 4 to 2 encoder circuit.*

| $D_3$ | $D_2$ | $D_1$ | $D_0$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |

**3.2. Priority Encoder Circuit**

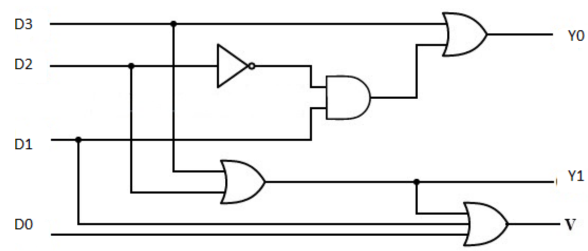
The encoders described so far will function properly if only one of the input lines is kept high. But sometimes, it may so happen that more than one input may be in advertently held high in an encoder. In that case, the prediction of output becomes difficult.

Fig. 5 shows the 4 inputs D0, D1, D2 and D3, 2 outputs Y1 and Y0 Priority encoder circuit. The circuit responds to the inputs based on the priority values assigned to the inputs. The most common priority encoder system is based on the highest decimal value in the input which is kept high.

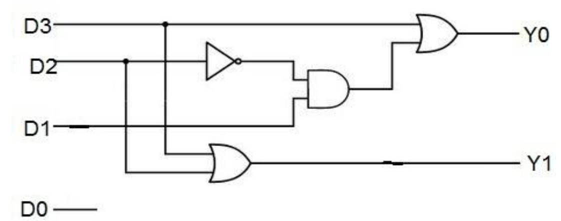
In a 4 to 2 priority encoder input D3 has the highest priority, so if D3 is high; output will be 11 regardless of the status of other input lines. Next D2 has the highest priority after D3, so when it becomes high and D3 is 0 the output will be 10 completely neglecting the other inputs. Next D1 is high and D3 and D2 is with 0 inputs, output is 01 neglecting the input for D0. Therefore $D_0$ is left alone as it is in low priority and for that it has no effect on the output. So it can be illustrated from the truth Table 2 if both D0 and D2 become high, the output will be 10 or decimal 2, because it assigns the D2 line of higher priority than D0 line and shows the output on higher priority line, completely neglecting lower priority line(s). Input D3 has the highest priority, so if D3 is high; output will be 11 or decimal 3 regardless of the status of other input lines. When D0 is 1 output is 00 in other cases D0 can be 1 or 0 but it will have no effect on priority encoder and for that reason it kept separate in the design. Here output V indicates the inputs validity.

The output for the circuit is given as below

$$Y_0=D_3+D_2{}' D_1$$
$$Y_1=D_3+D_2.$$




*(a)*




*(b)*

***Figure 5.*** *(a) 4 to 2 Priority Encoder circuit diagram (original) (b) In Priority Encoder D0 input left high (modified).*

***Table 2.*** *Truth table of 4 to 2 priority encoder circuit.*

| $D_3$ | $D_2$ | $D_1$ | $D_0$ | $Y_1$ | $Y_0$ | V |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 1 | 1 |
| 0 | 1 | X | X | 1 | 0 | 1 |
| 1 | X | X | X | 1 | 1 | 1 |

### 3.3. Octal to Binary (8 to 3) Encoder

An Octal to binary encoder accepts 8 input lines and produces 3-bit output based on the activated input line. Here the input lines range from $D_0$ to $D_7$ and output is a 3-bit binary code ($Y_2$ $Y_1$ $Y_0$). The circuit diagram and the truth table of an octal to the binary encoder are shown below in Fig. 6 and in table 3.

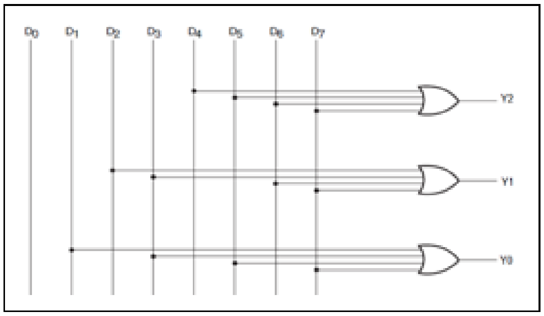



***Figure 6.*** *8 to 3 encoder circuit diagram.*

***Table 3.*** *Truth table of 8 to 3 encoder circuit.*

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Y2 | Y1 | Y0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

From the truth table, it can be deduced that the most significant output bit ($Y_2$) will be 1 when any of $D_4$, $D_5$, $D_6$, and $D_7$ is high.

Therefore,

$$Y_2 = D_4 + D_5 + D_6 + D_7$$

In the same way,

$$Y_1 = D_2 + D_3 + D_6 + D_7$$

$$Y_0 = D_1 + D_3 + D_5 + D_7$$

## 4. QCA IMPLEMENTATION OF DIFFERENT ENCODER CIRCUITS

Fig.7 shows the QCA layout of 4 to 2 Encoder circuit using QCAdesigner tool and Fig.8 shows the simulated output of the circuit. QCA based circuit layout of 4 to 2 Priority Encoder circuit and simulated output is shown in Fig.9, Fig. 10 and Fig. 11 shows the octal to binary encoder circuit using the same tool and the corresponding simulated output.

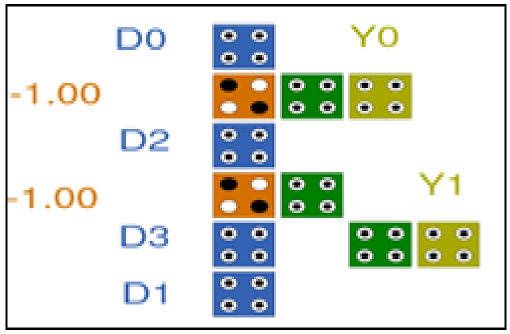



***Figure 7.*** *QCA layout of 4 to 2 encoder circuit.*

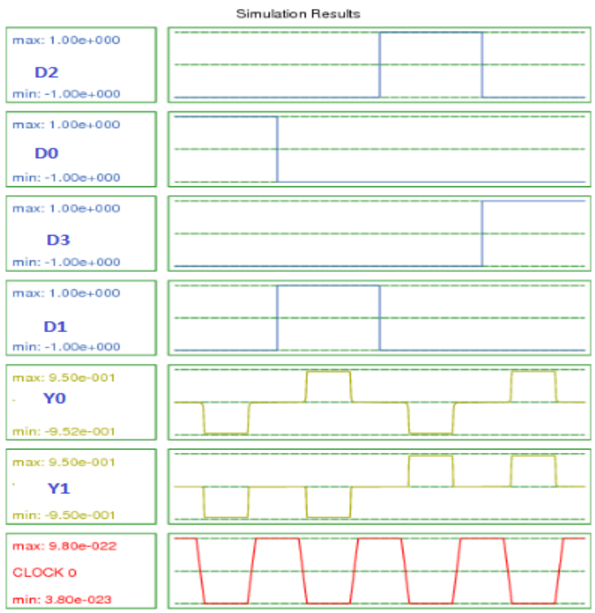
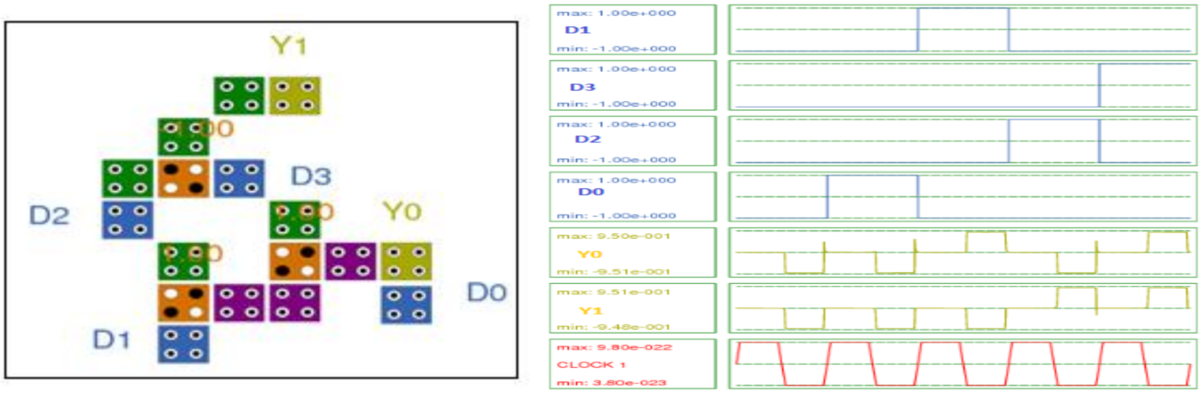



***Figure 8.*** *Simulated output of 4 to 2 Encoder circuit.*




*(a)* *(b)*

***Figure 9.*** *(a) QCA layout of 4 to 2 priority encoder circuit (b) Simulated output of 4 to 2 priority encoder circuit.*

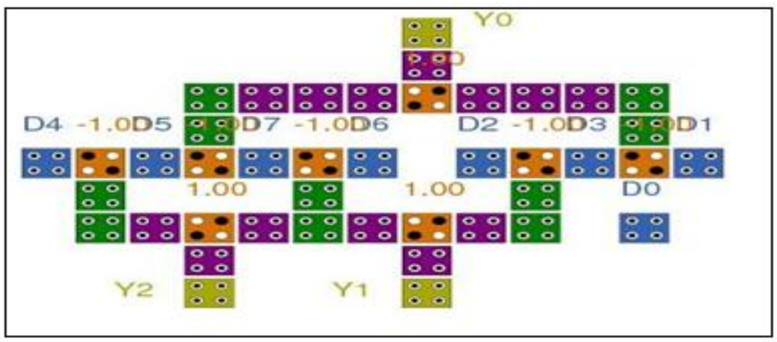



***Figure 10****. QCA layout of octal to binary encoder circuit.*

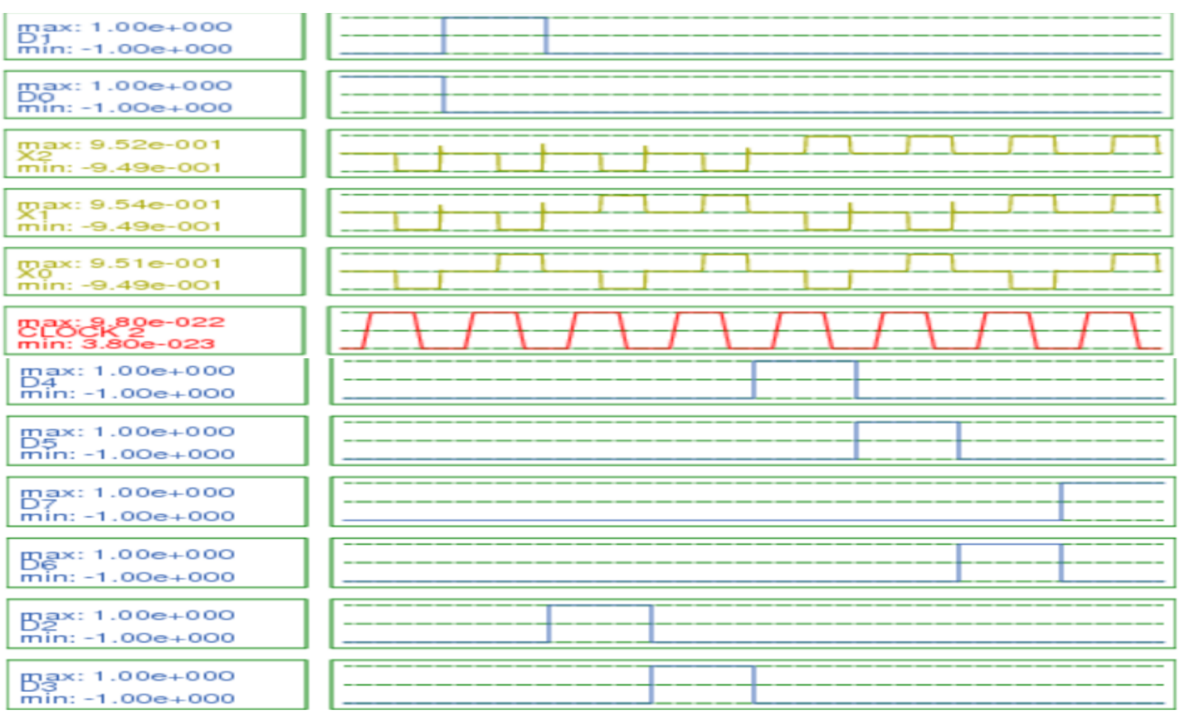



***Figure 11.*** *Simulated output of octal to binary encoder circuit.*

Table 4 shows the simulated output results for the above encoder circuits designed with QCA designer tool.

***Table 4.*** *Cell count, area, length, breadth & latency of simulated Encoder Circuits.*

| Device Name | Length (in nm) | Breadth (in nm) | Cell Count | Area (in $nm^2$) | Operation Cost | Latency | No of Gates |
|---|---|---|---|---|---|---|---|
| 4 to 2 Encoder | 136 | 78 | 11 | 21170 | 0.3928 | 0.25 | 2 |
| 4 to 2 Priority Encoder | 138 | 122 | 17 | 24764 | 0.4047 | 0.5 | 3 |
| Octal to binary Encoder | 178 | 255 | 42 | 50416 | 0.3589 | 0.5 | 8 |

## 5. COMPARATIVE STUDY WITH THE PREVIOUS DESIGNS

Proposed encoder designs using layered NAND and NOR gates reduced the cell numbers and total cell area coverage dramatically compare to the previously suggested designs. Table 5 shows the comparative study of different priority encoder circuits designed previously. It is established that the proposed design takes only 17 cells to design the circuit where as existing designs in the papers [15], [16], [18] and [19] used 178, 100, 40 and 165 cells respectively to design the same circuit. It is seen from the table that the proposed design consumes less area compare to the existing designs.

The comparative analysis with the previous designs of Octal to Binary Encoder is shown in Table 6 and compared with the designs [16] and [17]. Table 7 shows the same for 4 to 2 Encoder circuit where only 11 cells are required to realize the circuit where the coverage area is 21170 $nm^2$ compare to the paper [19] with area consumption of 198000 $nm^2$.

***Table 5.*** *Comparison of proposed priority encoder design with existing designs.*

| Design Reference | No. of cells | Area required($nm^2$) |
|---|---|---|
| Design as in [14] | 183 | 292042.14 |
| Design as in [15] | 178 | 210000 |
| Design as in [16] | 100 | 130000 |
| Design as in [18] | 40 | 50820 |
| Design as in [19] | 165 | 198000 |
| Proposed Design | 17 | 24764 |

***Table 6.*** *Comparison of proposed octal to binary encoder design with existing designs.*

| Design Reference | No of cells | Area required($nm^2$) |
|---|---|---|
| Design as in [16] | 281 | 66000 |
| Design as in [17] | 79 | 130000 |
| Proposed Design | 42 | 50416 |

***Table 7.*** *Comparison of proposed 4 to 2 encoder design with existing designs.*

| Design Reference | No of cells | Area required($nm^2$) |
|---|---|---|
| Design as in [19] | 165 | 198000 |
| Proposed Design | 11 | 21170 |

Studying the above comparative designs from table 5, 6 and 7 the proposed designs are proved to be better than their predecessor in terms of the number of cells required and the area to realize the circuit.

## 6. POTENTIAL ENERGY OF ENCODER CIRCUITS FOR DIFFERENT INPUT STATES

In Quantum Dot Cellular Automata, the cells are connected with one another. In each cell, there exist two electrons separated diagonally by a fixed distance. This configuration is made to avoid Coulomb repulsion force. For practical calculation, it is assumed that dimensions of all cells are same.

In QCADesigner software, width and height of each QCA cell is 18 nm and the dot diameter is 5 nm and inter-cell spacing is 2 nm. For simplicity of calculation, it is assumed that only neighboring cells have an influence in determining the potential energy. Therefore, in this way, the total potential energy of the design can be found for different input combinations. It is well known that for stability, the electrons should be aligned in such a way so as to reduce the potential energy as much as possible. The input state with least potential energy is the most stable and suitable for QCA operation [21].

In QCA potential energy of a circuit always varies with respect to its input states and polarizations. Fig. 12 shows the distance of a dot from its neighboring electrons. The state with minimum potential energy is said to be the inputs are given below in the following Fig.13, Fig.14 and Fig.15. Table 8 shows the potential energy calculations for different encoder circuits designed in this paper. Potential energy between two electrons is given by the equation 2,

$$U=(k\,q1\,q2)/r \qquad (2)$$

where $kq1q2 = 9\times10^{9} \times (1.6)^{2} \times 10^{-38}$
$=23.04\times10^{-29} = A$

here $k$ is the fixed colon, $q1$ and $q2$ are the electron charges and $r$ is the distance between two electrons [22, 23, 24] and it is the radius of effect. By putting the values of $k$ and $q$, kink energy is calculated and it varies inversely with distance r. The energy should be minimum for the circuit to be a robust one. Summation of U values calculated by the equation 2 gives the kink energy. Calculations of potential energy for different input signals are shown with bar charts and the estimated minimum energy is also shown for the reliable output. Kink energy calculation for a PFD circuit is explained in [25].

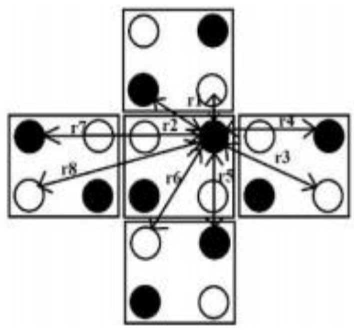



***Figure12.*** *Distance of a electron from its neighboring electrons denoted as r1, r2 etc.*

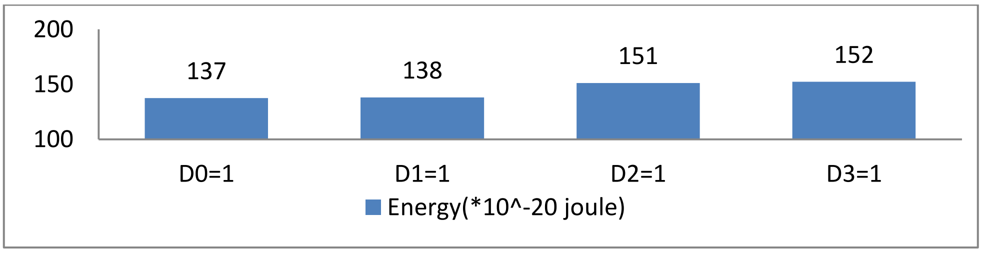



***Figure13.*** *Potential energy of 4 to 2 encoder circuit for different input states.*

***Table 8.*** *Potential energy of encoder circuits for different input states.*

| Input States | | | | Output States | | Potential Energy in Joule (multiplying factor $10^{-20}$) |
|---|---|---|---|---|---|---|
| 4 to 2 Encoder | | | | | | |
| D3 | D2 | D1 | D0 | Y1 | Y0 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 137.488 |
| 0 | 0 | 1 | 0 | 0 | 1 | 138.066 |
| 0 | 1 | 0 | 0 | 1 | 0 | 151.212 |
| 1 | 0 | 0 | 0 | 1 | 1 | 152.264 |
| 4 to 2 Priority Encoder | | | | | | |
| D3 | D2 | D1 | D0 | Y1 | Y0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 251.236 |
| 0 | 0 | 0 | 1 | 0 | 0 | 251.236 |
| 0 | 0 | 1 | 0 | 0 | 1 | 230.784 |
| 0 | 0 | 1 | 1 | 0 | 1 | 230.784 |
| 0 | 1 | 0 | 0 | 1 | 0 | 258.232 |
| 0 | 1 | 0 | 1 | 1 | 0 | 258.232 |
| 0 | 1 | 1 | 0 | 1 | 0 | 252.538 |
| 0 | 1 | 1 | 1 | 1 | 0 | 252.538 |
| 1 | 0 | 0 | 0 | 1 | 1 | 272.166 |
| 1 | 0 | 0 | 1 | 1 | 1 | 272.166 |
| 1 | 0 | 1 | 0 | 1 | 1 | 280.186 |
| 1 | 0 | 1 | 1 | 1 | 1 | 280.186 |
| 1 | 1 | 0 | 0 | 1 | 1 | 305.9 |
| 1 | 1 | 0 | 1 | 1 | 1 | 305.9 |
| 1 | 1 | 1 | 0 | 1 | 1 | 300.206 |
| 1 | 1 | 1 | 1 | 1 | 1 | 300.206 |

| Octal to Binary Encoder | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Y2 | Y1 | Y0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 602.984 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 580.471 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 558.085 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 576.111 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 643.46 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 630.088 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 595.483 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 610.115 |

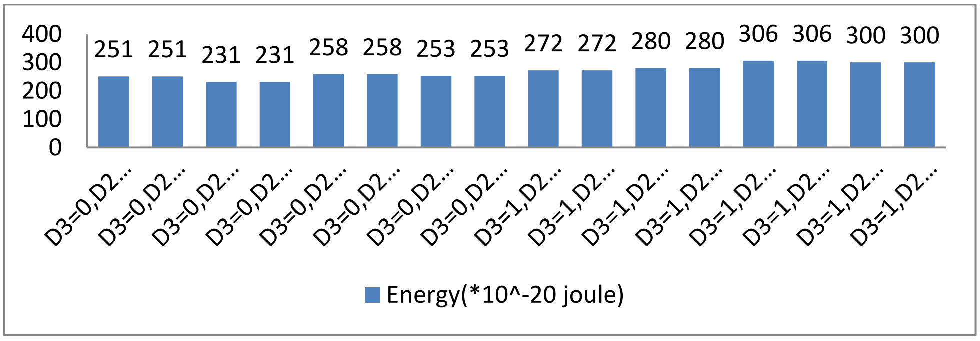



***Figure 14.*** *Potential energy of priority encoder circuit for different states.*

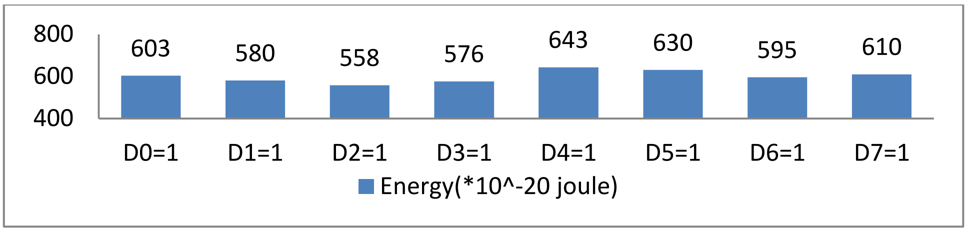



***Figure 15.*** *Potential energy of octal to binary encoder.*

## 7. CONCLUSION

From the simulations, two inferences can be drawn. First of all, using the universal gate logic the number of cells and area required to design different encoder circuits are reduced dramatically without sacrificing the efficiency. However there is not much design for the 4 to 2 encoder circuits with QCA technology.

Secondly, using the conventional methods for the calculations of potential energy the encoder circuits for different possible input combinations have been calculated and are rounded off to their closest possible integer values. These values are represented using bar-graphs in Section 6. As it has been already mentioned that the input state with the least potential energy is best suitable for QCA operation, the most stable input state can be found from the graphs. From Fig 13 for 4 to 2 Encoder circuit, that stable state occurs when D0 is 1. Similarly, from Fig 14 for Priority Encoder circuit, the states with D1 as 1 and all higher bits are zero are considered to be the most stable state. For Octal to Binary Encoder circuit which is shown in Fig 15, D2 equal to 1 is the most stable state.

## 8. DISCUSSION AND FUTURE SCOPE

This paper discussed the detail design and implementation of 4 to 2 encoder, 4 to 2 priority encoder and 8 to 3 encoder circuits using layered NAND and NOR gate. All the simulations are done using the QCADesigner software tool [26]. The designs give the information about the total area requirement and the number of cell count.

The designs have also been compared with their predecessors. Furthermore, potential energy for each design for each input states have been calculated to find the most suitable state of operation. We conclude QCA technology as one of the most promising technologies in the field of nano-science and nano technology. It can be one of the leading technologies in quantum computation. In the QCA technology the opportunity to set the operating frequency and propagation delays are not there but can be an important parameter for further research. The main objective of this paper is to find an optimum design of encoder circuits in terms of cell number and size without sacrificing their efficiency and valid output.

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