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Exploring and Exploiting Quantum-Dot Cellular Automata

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Abstract

The Full Adders (FAs) constitute the essential elements of digital systems, in a sense that they affect the circuit parameters of such systems. With respect to the MOSFET restrictions, its replacement by new devices and technologies is inevitable. QCA is one of the accomplishments in nanotechnology nominated as the candidate for MOSFET replacement. In this article 4 new layouts are presented for FA; implemented as two at one layer and the other two at three layers; this is performed in a step by step manner and by providing the details and introducing each one's problems. The layout process continues till an optimized layout is obtained. The layout and correct assessment of the introduced circuit function is accomplished by using QCA Designer simulation tool. The comparison of the results obtained through simulation confirms that the third design is better than other three designs with respect to cell count and area.

Keywords: *Full adder, Nanotechnology, QCA*

1. INRODUCTION

Adding is one of the most fundamental operations in arithmetic through which more complicated arithmetic circuits like Multiplication, Division and Exponentiation could be executed [1] since in these complicated calculations addition circuits are widely applied. Ever since the digital systems and arithmetic circuits evolved, vast studies have been conducted on the adders as of now and on. As the efficiency in Adder function is promoted, the parameters of the integrated circuits derived from them could be upgraded [2]. A few of these parameters are delay, consumable power and complexity. The Adder function is a vital element of the processers due to its use scope as well as its application in arithmetic logic units, floating-point arithmetic units and address generation providing access to the cache and the main memory [3]. Thus, the execution of this arithmetic function should be fast and low powered in order to construct rapid and low-powered chips, an undeniable necessity. Here it should be noted that an increase in Adder efficiency function is one of the biggest challenges facing the design and execution of the arithmetic circuits.

The MOSFET transistors and the CMOS technology are assigned the biggest portion to digital circuit's execution, which have vast contribution in manufacturing of useful devices like computers, mobile phones, digital cameras and other electronic components. The major advance in this technology is attributed to the reduction in transistor size. This size reduction increases the number of the transistors in a chip; hence, promoting the chip capabilities and realization of the Moore's Law. Considering Moore's low, the following question comes to mind: How far can this size reduction go on? With respect to the ongoing advances in physics and chemistry sciences this pattern is facing big challenges. In a sense, this size reduction is facing serious restrictions like increased leakage currents, difficulty on increase of ON-current, large parameter variations, low reliability and yield and increase in manufacturing cost [4]. This fact makes the studies on replaceable devices and technologies an inevitable

issue. Some of the introduced devices and technologies are: CNFET [5, 6], spin wave architecture, single electron devices and quantum-dot Cellular Automata (QCA) [7, 8]. The QCA is not only one of the novelties of nanotechnology by having good properties based on its nanoscale, but is a new method in implementing digital circuits and transferring data [9, 10]. The generality and efficiency of this technology have been investigated by researchers [11-14]. Many design implementation are executed through QCA and in different articles, the execution of the circuits through this technology is expressed regarding: Carry-look ahead adder, barrel shifter, microprocessor, prefixed Adder and Filed Effect Programmable Gate Arrays (FPGAs) [8, 11, 11-17].

One of the problems with QCA is the fact that the general delay and functioning manner of the layout circuit depends on its own layout [18]. For this purpose, here, the application of the QCA technology is assessed for designing and implementing full-adder: 4 new layouts are presented for full-adders; implemented as two at one layer of cells and the other two at three layers of QCA cells; this is performed in a step by step manner and by providing the details and introducing each one's problems. The layout process continues till an optimized layout is obtained. The QCA can be implemented through the following four approaches [18]:

1- Metal QCA [19]: The base cell field is of silicon-oxide containing 6 metal lines, which play the quantum dots' role. The electrons among the adjacent dots can be interchanged. Of course this cell can function well at temperatures close to zero.

2- Semiconductor QCA [20]: In this approach the low temperature prevails as well and for increasing the temperature in the working mode the cell size must be reduced, the potential of which is very low nowadays. In this approach all cells must be uniform.

3- Molecular QCA [13]: This QCA contains a series of molecules which play the quantum dots' role. The advantages of these molecules are: uniformity, accurate function at room temperature, switching speed and small size. This QCA approach is implementable.

4- Magnetic QCA [21-23]: The second type of implementable QCA that functions at room temperature. Each one of its cells has two logic values, of one and zero. Of course the main drawback is its low speed, even slower than Molecular QCA and CMOS. The advantages here are: low power consumption and ability to be produced through the contemporary technologies.

2. RELATED WORKS

In the article [24], with the use of an algorithm, the authors introduced a full adder cell employing three majority and two inverter gates. The QCA-based FA designs presented in [12] are implemented only in one layer (see Figure 1 (b)) using proper clocking to reduce the noise impact. By employing special features of QCA such as propagation of information on QCA wires, a carry flow adder is introduced in [25]. The simulated results are compared with that of a carry look ahead adder. The comparisons show the superiority of the carry flow adder against the CAL adder. This adder is depicted in Figure 1 (c). In another article, five input majority gate is introduced in order to reduce the number of gates and cells in implementing QCA functions. The corresponding FA introduced in [26] is shown in Figure 1 (d). Two full adder cells are presented in [27], the first one is designed in one layer and the second one is implemented in three layers. To implement these full adders five input majority gates are employed. Another QCA full adder cell which uses five input majority gates is presented in [28]. The number of clock in this article is ½ and the number of cells are 31. Since the majority gates are the foundation of QCA design procedure, in

[29] reconfigurable majority gates of five and seven inputs are presented. Using the presented majority gates, a full adder is implemented. In another research a robust single layer wire crossing method has been introduced in [30]. Using their method only requires one type of cells and to design on one surface there is no need to rotate any cells. By employing the method suggested, they presented parity generator, full adder and compressor circuits.

3. THE PROPOSED FULL ADDERS

Here, the proposed Full Adders are introduced, implemented and simulated through QCA Designer tool [14]. The first and second designs are implemented at one layer and the third and fourth designs are implemented in three layers.
The relation among the inputs and outputs in a FA are expressed as follows:

$$Sum=abc_{in}+\bar{a}\bar{b}c_{in}+\bar{a}b\overline{c_{in}}+a\bar{b}\overline{c_{in}} \quad (1)$$

$$Carry=ab+ac_{in}+bc_{in} \quad (2)$$

Equation (2) is similar to Majority function which is used to compute the carry output of the FA. To implement equation (1) with the least number of gates it can be modified as follows [24]:

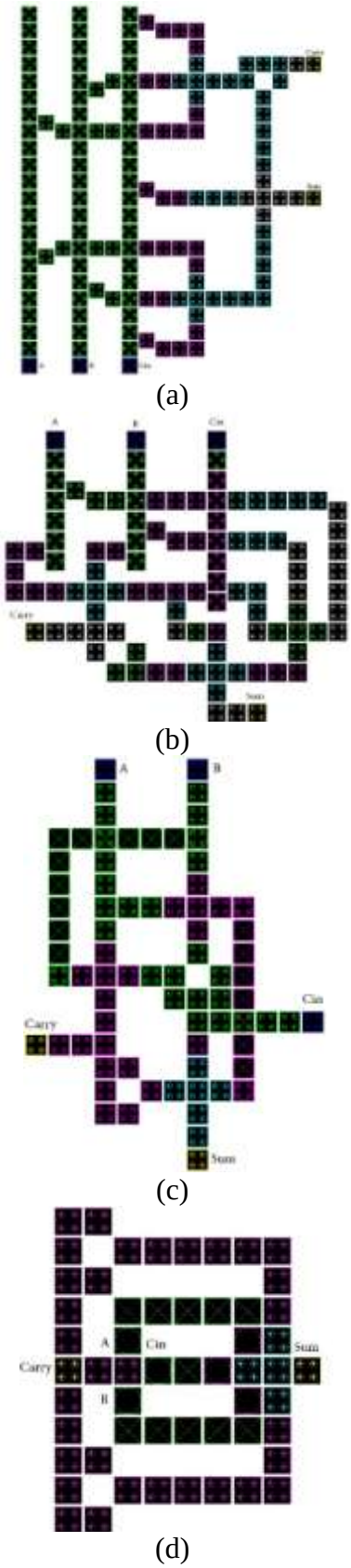
$$\begin{aligned}Sum&=C_{in}\bar{a}\bar{b}+C_{in}ab+a\bar{b}\overline{C_{in}}+\bar{a}b\overline{C_{in}}\\&=\left(C_{in}\bar{a}+C_{in}\bar{b}\right)\left(C_{in}\bar{a}\right)\left(C_{in}\bar{b}\right)+C_{in}ab\\&+\left(\bar{a}\bar{b}+\bar{a}\bar{b}\overline{C_{in}}+\bar{b}\overline{C_{in}}+\bar{a}\overline{C_{in}}\right)\left(ab+a\overline{C_{in}}+b\overline{C_{in}}\right)\\&=C_{in}\left(\left(\bar{a}+\bar{b}\right).\left(\bar{a}+\overline{C_{in}}\right).\left(\bar{b}+\overline{C_{in}}\right)\right)+C_{in}(ab\\&+a\overline{C_{in}}+b\overline{C_{in}})+\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right)\\&\left(ab+a\overline{C_{in}}+b\overline{C_{in}}\right))\\&=M(C_{in},((\bar{a}+\bar{b})(\bar{a}+\overline{C_{in}})(\bar{b}+\overline{C_{in}}))\\&,(ab+a\overline{C_{in}}+b\overline{C_{in}}))\\&=M(C_{in},\overline{(ab+aC_{in}+bC_{in})},(ab+a\overline{C_{in}}+b\overline{C_{in}})\end{aligned}$$

$$Sum=M(C_{in},\overline{M(a,b,C_{in})},M\left(a,b,\overline{C_{in}}\right)) \quad (3)$$

On the one hand since $\overline{Carry}=\overline{M(a,b,C_{in})}$, equation (3) can be expressed as:

$$Sum=M(C_{in},\overline{Carry},M\left(a,b,\overline{C_{in}}\right)) \quad (4)$$

For the first, second and third introduced designs, equations (2) and (4) are used. The schematic diagram of the designs first to the third is depicted in Figure 2.



(a) (b) (c) (d)

Figure1. *Previous FA designs*

According to Figure 2 for implementation of the first three proposed designs three Majority gates and two inverter gates are of need. The QCA structures of the first and second designs are shown in Figures 3 and 4, respectively.

The wire length of the input A is very long (see Figure 3). In fact, many cells are fit in clock zone 1. The delay in QCA circuit is subject to the available cells in every clock zone. The more the cells count are, the more the circuit delay [25]. To eliminate this problem, the second design is being proposed. The structure of the second FA is modified in a way that would decrease the number of the cells in every clock phase.

The first and second proposed designs are executed at one level. This phenomenon leads to enlargement of the circuit.

In order to eliminate the destructive effect of the interaction of the neighboring cells there must be at least a distance of two cells among every two signals. Similar to the two previous designs the third design is another way of implementing equations (2) and (4). Here, unlike the two previous designs the third design is implemented at three layers. The third proposed design is illustrated in Figure 5.

In the three proposed designs, three Majority and two inverter gates are applied as yet. In the fourth design the attempt is made to reduce the numbers of gates.

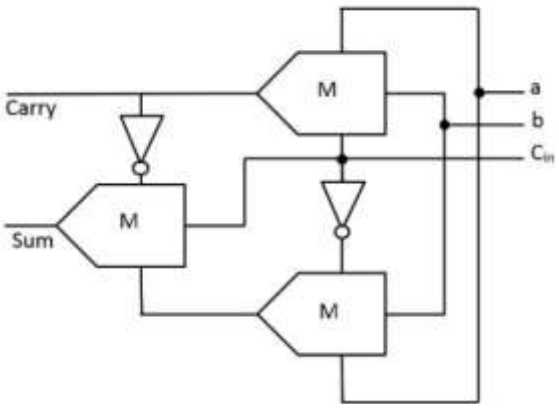


Figure2. *The schematic diagram of the design I and II*

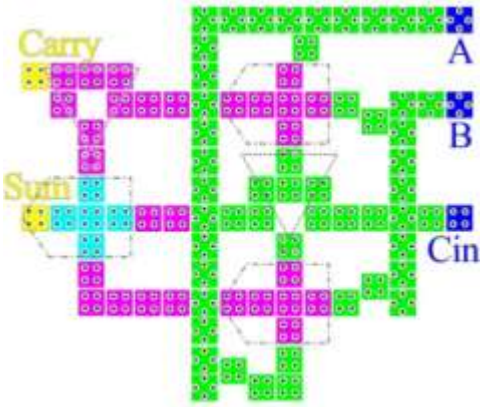


Figure3. *Proposed design I*

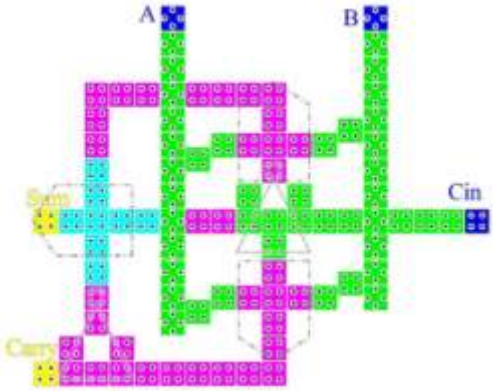


Figure4. *Proposed design II*

The equation (4) can be conducted in a way that in designing the Full Adder one of the inverter gates is eliminated [8]:

$$
\begin{aligned}
\mathrm{Sum} &= \bar{a}\bar{b}C_{in}+\bar{a}b\overline{C_{in}}+a\bar{b}\overline{C_{in}}+abC_{in} \\
&= \left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}}\right)\left(\bar{a}b\overline{C_{in}}+\bar{a}\bar{b}C_{in}\right. \\
&\left.+bC_{in}\right)+\left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}}\right)a \\
&+\left(\bar{a}b\overline{C_{in}}+\bar{a}\bar{b}C_{in}+bC_{in}\right)a \\
&= M\left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}},\bar{a}b\overline{C_{in}}+\bar{a}\bar{b}C_{in}\right. \\
&\left.+bC_{in},a\right) \\
&= M\left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}}\right. \\
&\left.,\left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}}\right)b\right. \\
&\left.+\left(\bar{a}\bar{b}+\bar{a}b\overline{C_{in}}+b\overline{C_{in}}+\bar{a}\overline{C_{in}}\right)C_{in}+bC_{in},a\right) \\
&= M\left(\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right)\right. \\
&\left.,\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right)\right. \\
&\left.b+\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right)C_{in}+bC_{in},a\right) \\
&= M\left(\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right),\right. \\
&\left.M\left(\left(\left(\bar{a}+\bar{b}\right)\left(\bar{a}+\overline{C_{in}}\right)\left(\bar{b}+\overline{C_{in}}\right)\right),b,C_{in}\right),a\right) \\
&= M\left(\left(\overline{ab+aC_{in}+bC_{in}}\right),\right. \\
&\left.M\left(\left(\overline{ab+aC_{in}+bC_{in}}\right),b,C_{in}\right),a\right) \\
&= M\left(\overline{M(a,b,C_{in})},M\left(\overline{M(a,b,C_{in})},b,C_{in}\right),a\right) \\
\mathrm{Sum} &= M\left(\overline{\mathrm{Carry}},M\left(\overline{\mathrm{Carry}},b,C_{in}\right),a\right) \qquad (5)
\end{aligned}
$$

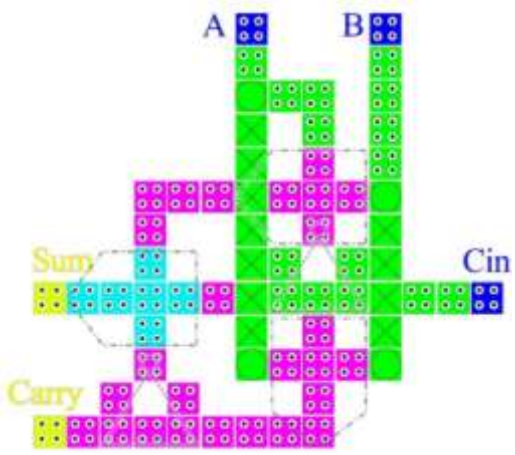


Figure5. *Proposed design III*

The idea behind execution of the fourth design lies in equations (2) and (5). Consequently, this circuit consists of three Majority gates and one inverter gates. The schematic diagram of the fourth design is presented in Figure 6. It should be noted that inverter gate implementation compared to Majority gate implementation imposes more hardware cost on the circuit; therefore, it is expected that fourth implementation would have less hardware cost and less delay. The structure of the fourth proposed QCA design FA is shown in Figure 7. Here, unlike what was expected, one gate reduction has led to an increase in hardware cost and delay time.

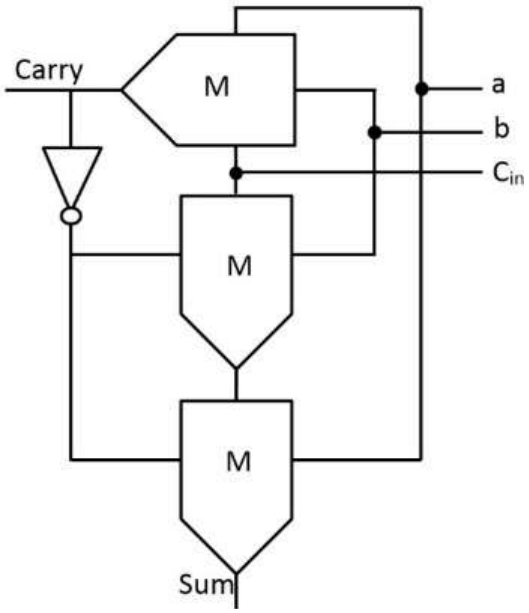


Figure6. *The schematic diagram of the fourth design*

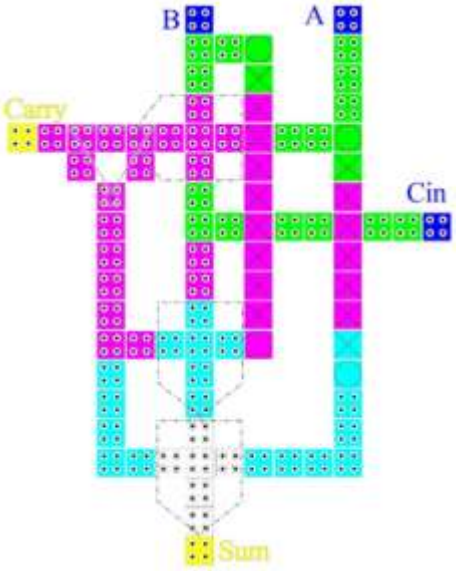


Figure7. *Proposed design IV*

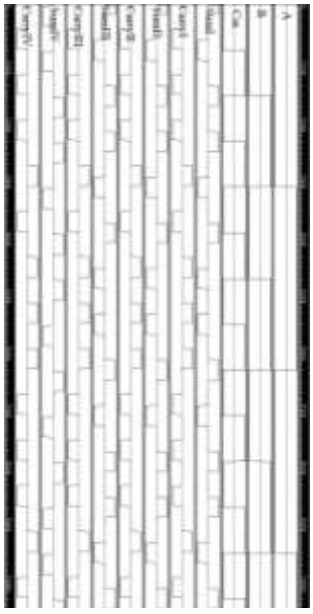


Figure13. *The results obtained from the four proposed designs*

Table1. *The results of simulation including cell number, area, layer and delay*

Design	Cells	Area (μm×μm)	Layers	Delay
design I	89	0.31×0.27	1	¾
design II	90	0.35×0.27	1	¾
design III	78	0.27×0.25	3	¾
design IV	93	0.29×0.37	3	1
[12]	102	0.36×0.31	1	2
[25]	86	0.26×0.35	3	¾
[8]	80	0.22×0.32	3	1
[24]	145	0.36×0.44	1	1
[32]	69	0.26×0.32	1	1

4. SIMULATION AND COMPARISON

Simulation has been performed on previous designed adders and then the results are compared with the proposed designs (I, II, III, and IV).

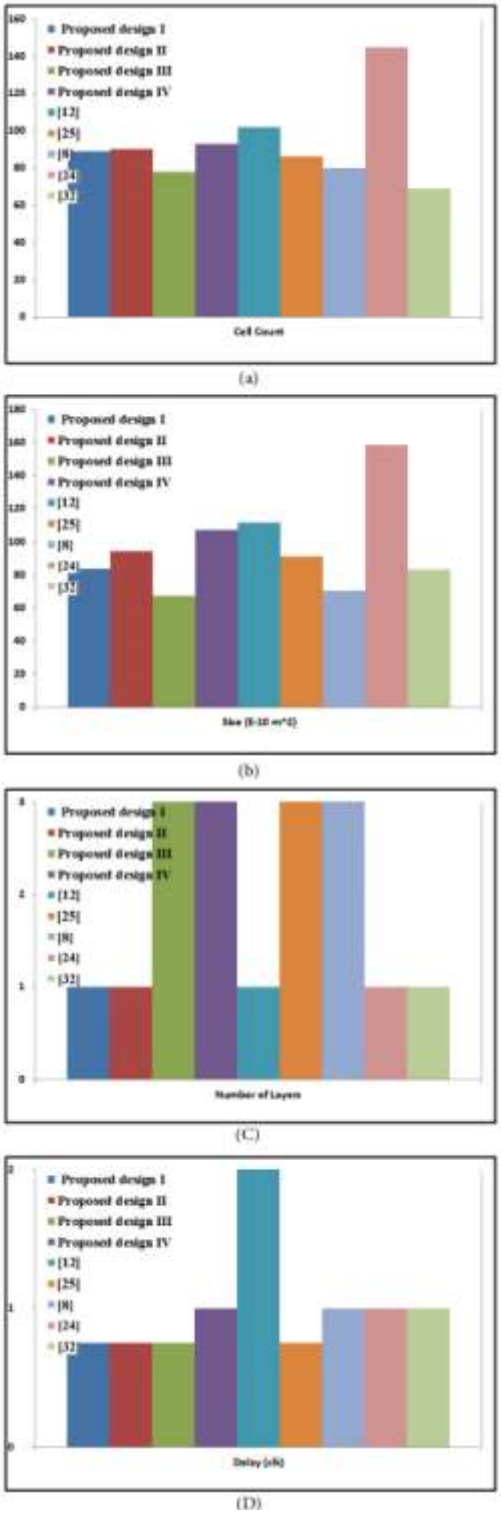


Figure14. *Graphical simulation results (a) cell count, (b) area, (c) layers and (d) delay*

The design layout and execution of the proposed circuits are performed through QCA Designer software. The dimensions of every cell are 18nm, the well Quantum Dot is 5nm and the distance of neighboring cell (center-center) is 20 nm.

The implementations are completed through Bistable Approximation simulating engine. The measurements of cell count, area, number of layers and delay of previous works and the new four proposed adders are presented in Table 1 for the purpose of comparison.

The simulation results of the robust QCA full-adder designs are depicted in Figure 8 where the outputs are determined in the order of each design number. That is, sum1 and carry1 represent the outputs of proposed design I, and so on, and at last sum4 and carry4 are the output wave forms of proposed design IV.

Since in FA presented by [26] in some specific patterns of inputs the outputs are not accurate and according to [31], feeding inputs of the circuit is impossible, therefore, the comparison against [26] has not been carried out.

It is apparent that among the existing FAs the multi-level proposed design III has better cell count with ¾ clk and occupies less area compared with other full adders. The cell count of proposed designs and previous works are shown in Figure 9 (a), the area comparison is depicted in Figure 9 (b) and the number of layers and also the delay of proposed designs are shown in Figure 14 (c) and (d), respectively.

5. CONCLUSION

The full adders are among the fundamental elements in digital systems. Their optimized implementation has a direct influence on the circuit parameters derived from them. Now that the once prevailing silicon industry is facing restrictions the research on devices and materials has gained specific importance. In this article four new FA are designed and executed through the QCA technology. The first two proposed designs are

implemented at one layer and the next two are implemented at three layers. Each one of the introduced designs is simulated and their functionality is verified through the QCADesigner simulator. The comparison of the obtained results from simulators indicates that the third proposed design is more efficient.

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