Int. J. Nanosci. Nanotechnol., Vol. 19, No. 1, March 2023, pp. 9-19
DOI: 10.22034/ijnn.2023.1988468.2327

A Technique, Based on Thevenin Equivalent Method, to Study the Noise Performance of Analog Circuits Involving both CNTFET and MOS Devices

Roberto Marani[1] and Anna Gina Perri[2,*]

[1]Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy, 70125, Bari, Italy
[2]Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, 70126, Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
(Received: 26 January 2023 and Accepted: 17 February 2023)

Abstract

This paper presents a procedure, based on Thevenin equivalent method, to analyse the noise effects in analog circuits based on CNTFET and MOS devices. To achieve this goal, we use a semi-empirical compact CNTFET model, already proposed by us, including noise source contributions, and the BSIM4 model for MOS device. After a brief review of these models, as example of analog circuit, the proposed procedure is applied to study a basic current mirror and the simulation results allow to determine easily the different noise contribution of every single source. The software used is Advanced Design System (ADS) which is compatible with the Verilog-A programming language.

Keywords: *CNTFET, MOSFET, Modelling, Noise Effects, Analog circuits, Advanced Design System.*

1. INRODUCTION

One of the main differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon [1].

For conventional CNTFETs, utilized for high-performance and low-power memory designs [2-15], we have already proposed a compact, semi-empirical model [2-3], in which we introduced some improvements to allow an easy implementation both in SPICE and in Verilog-A [16].

Moreover, in [17], we have presented a procedure, based on Thevenin Equivalent method, to analyse the noise effects in analog circuits based on CNTFET devices. In particular in [17] the noise mechanisms have been discussed and the impact of the different noise sources analyzed.

In this paper we want to demonstrate that the same procedure can be also applied to study the noise performance of analog circuits involving MOS devices.

To aim this goal, for the MOSFET model, we use the BSIM4 one of ADS library. BSIM (Berkeley Short-channel IGFET Model) [18] refers to a family of MOSFETs for integrated circuit design.

As example, the proposed procedure is applied to design of a basic current mirror based on MOSFET device, like we did in [17], and the simulation results allow to determine easily the different noise contribution of every single source and to compare the noise performance of the CNTFETs and of the MOS devices.

The presentation is organized as follows:

Section 2 gives a brief review of CNTFET and MOSFET models used, recalling a compact noise model, already proposed by us in [19]. Then, in Section 3, we present the obtained results, together with the description of the setup-work used

during the simulations. Finally Section 4 gives the conclusions and future developments.

2. A BRIEF REVIEW OF CNTFET AND MOSFET MODELS

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them. It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact the most complex part of the model is contained in Verilog A.

In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [20], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT}, have the expressions reported in [2-3].

An exhaustive description of our C-V model is widely described in our References [14-15] and therefore the reader is requested to consult them, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are widely explained:

$$\begin{cases} C_{GD} = q\sum_{p}\dfrac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\dfrac{\partial n_{Dp}}{\partial \xi_{Dp}}\dfrac{\partial \xi_{Dp}}{\partial V_{CNT}}\dfrac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\dfrac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\dfrac{\partial n_{Sp}}{\partial \xi_{Sp}}\dfrac{\partial \xi_{Sp}}{\partial V_{CNT}}\dfrac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

Figure 1 shows our model, in which we have reported the values of circuital elements.

It is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

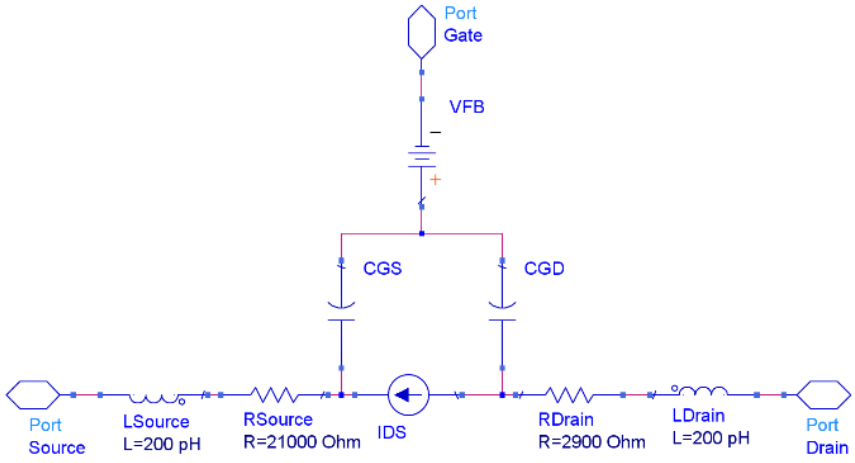

Figure 1. *Equivalent circuit of a n-type CNTFET.*

As already said, for the MOSFET model we use the BSIM4 model of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [18] refers to a family of MOSFETs for integrated circuit design. In this work BSIM4 has been used for the 32 nm technology nodes. The MOSFET parameters for BSIM4 model were obtained by Predictive Technology Model (PTM) web site from the Nanoscale Integration and Modelling Group of Arizona State University. In particular we have selected MOSFET sizes in order to

obtain output characteristics comparable to those of CNTFET.

Regards to the noise model, in [19] we have already proposed a compact noise model of CNTFET, and therefore, also in this case, we suggest the reader to consult the Reference [19].

Figure 2 recalls the proposed CNTFET noise model, including five different noise sources, which are [19]:

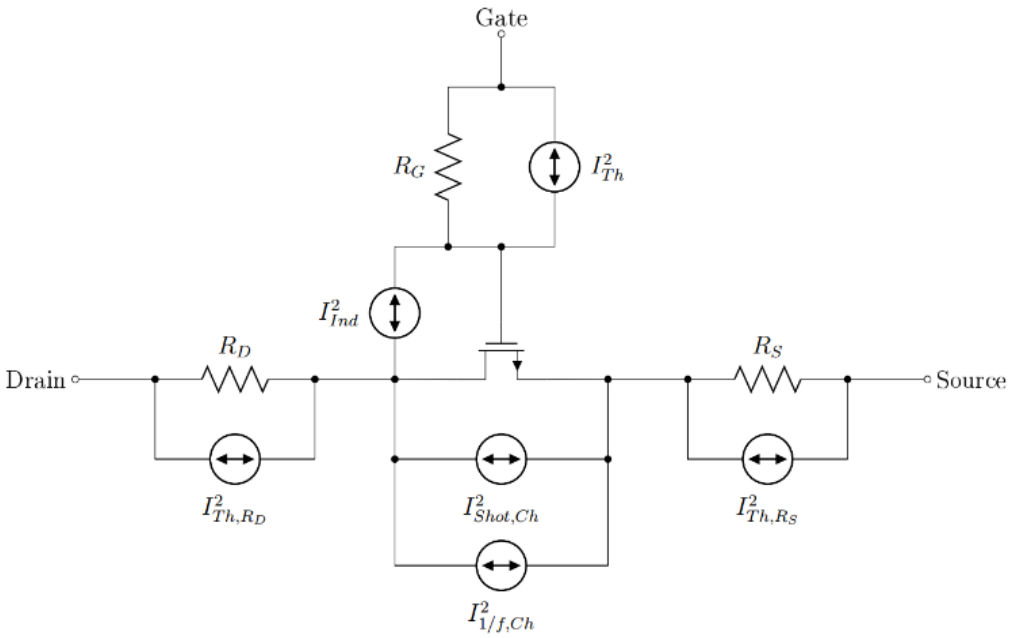

Figure 2. *CNTFET noise model [19].*

1) Thermal noise of R_G

The gate resistance R_G, implemented as a lumped element with a small value (~ 2 Ω), produces a thermal noise, whose power spectral density (PSD) is:

$$S_{Th,RG} = 4kT/R_G \quad (3)$$

For the implementation of this kind of noise, we used the built-in ADS feature [16] that evaluates thermal noise of resistors used in circuits.

2) Thermal noise of R_S and R_D

The tube end-regions highly doped show high resistances R_S and R_D (~ kΩ), and their contribution to the power spectral density is in agreement with Eqn. (3).

3) Channel thermal noise and shot noise

Conventional noise theory [21] for long-channel devices describes the power spectral density of drain noise as:

$$S_{Th,Ch} = 4kT\gamma g_{d0} \quad (4)$$

being g_{d0} the channel conductance at V_{DS} = 0 V.

The parameter γ is the so-called *white noise gamma factor*, depending on the operating status of the device and it is equal to 2/3 when CNTFET operates in saturation region.

This classical theory is not satisfactory for white noise in short-channel devices. In these devices it is necessary to consider a white noise gamma factor equals to 2 or 3 [22, 23].

The channel shot noise can be expressed as:

$$S_{Shot,Ch} = 2qI_{DS}.F(I_{DS}) \quad (5)$$

where $F(I_{DS})$, i.e. depending on I_{DS}, is called *Fano factor*. Its value is between 0 and 1.

We considered the worst case condition, i.e. F = 1, having considered successive injection events completely uncorrelated. This last assumption allows us to use the Verilog-A white noise function that models processes whose current value is

completely uncorrelated with any previous or future values.

4) Flicker noise

According to the empirical law in [24], we considered the flicker noise in CNTFETs, whose power spectral density is:

$$S_{1/f,Ch} = A_H \left(\frac{I_{DS}^2}{f} \right) = \left(\frac{\alpha_H}{n} \right) \left(\frac{I_{DS}^2}{f} \right) \quad (6)$$

From Eq. (6) A_H is the ratio of the material-dependent Hooge constant, a_H, and the number of carriers n in the channel. We have chosen the value of a_H equal to 10^{-4}, that is a standard number for un-optimized semiconductor.

5) Channel-induced gate noise

Another type of intrinsic noise that should be considered in CNTFETs is the *channel-induced gate noise*, whose power spectral density can be described as [21]:

$$S_{Ind} = 4kT\delta \left(\frac{\omega^2 C_{GS}^2}{5 g_{d0}} \right) \quad (7)$$

For ballistic devices we have assumed δ equal to 4/3, considering no type of correlation between noise sources.

3. PROPOSED PROCEDURE FOR NOISE ANALYSIS IN ANALOG CIRCUITS BASED ON CNTFET AND MOSFET

To illustrate the proposed procedure, based on Thevenin Equivalent method, we apply it to the design of a basic mirror.

Basic current mirror is a circuitry designed to duplicate the current through a diode-connected active device by controlling the current in another active device, thus keeping the output current constant irrespective of the loading.

An ideal current mirror is simply an inverting current amplifier with low input resistance and very high output resistance.

We considered basic current mirror as an equivalent Thevenin voltage source (V_N) with its series noise resistance (R_N). Thus, we duplicated the circuit including two different passive loads (R_A = 50 Ω for circuit A and R_B = 100 Ω for circuit B), as shown in Figure 3.

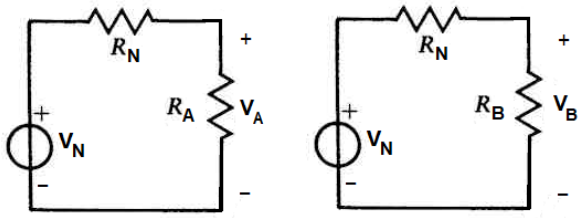

***Figure 3**. Equivalent Thevenin Noise circuits.*

Thanks to noise values of:

$$V_A = \frac{R_A}{R_A + R_N} V_N \quad \text{and} \quad V_B = \frac{R_B}{R_B + R_N} V_N$$

returned by the simulation, it has been possible to measure noise values of:

$$V_N = \frac{V_B V_A (R_A - R_B)}{V_B R_A - V_A R_B} \quad (8)$$

$$R_N = \frac{R_A R_B (V_A - V_B)}{V_B R_A - V_A R_B} \quad (9)$$

$$I_N = \frac{V_N}{I_N} = \frac{V_B V_A (R_A - R_B)}{R_A R_B (V_A - V_B)} \quad (10)$$

exclusively in all CNTFET (or MOSFET) mirror components.

Note that these expressions are valid if phase displacement, among components in design, is negligible.

For CNTFET the ADS circuits are shown in Figures 4 and 5.

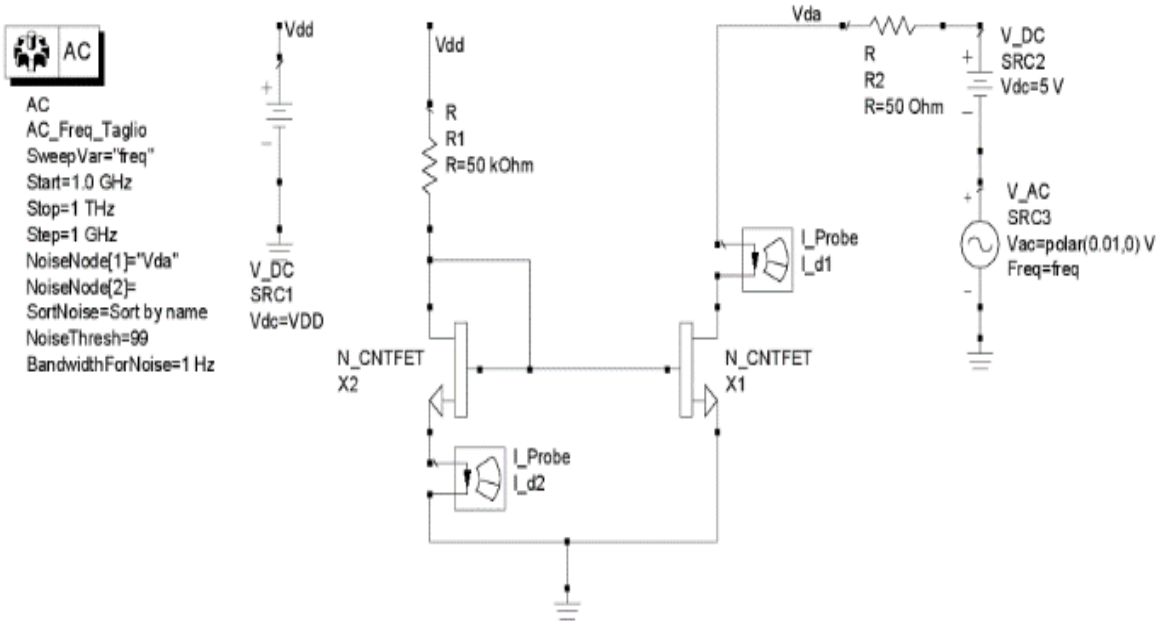

***Figure 4**. Design A of Noise simulation.*

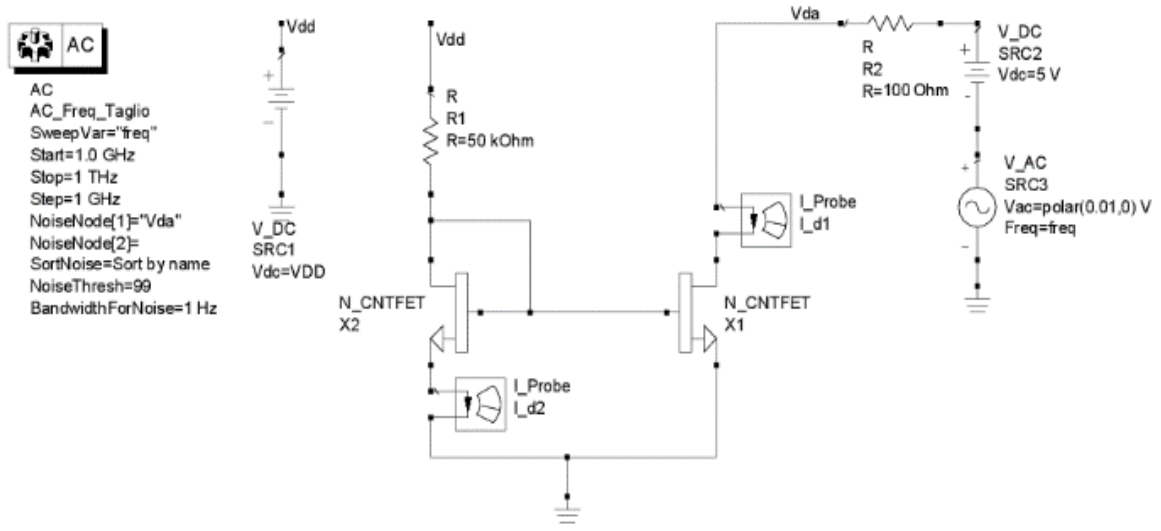

***Figure 5**. Design B of Noise simulation.*

In [17] we widely described this procedure for the analysis of noise in a CNTFET-based current mirror, and therefore we advise the reader to see this reference.

Therefore, in order not to burden the treatment, for a complete rating, we show all single voltage and current noise components (summed in quadrature for CNTFET1 e CNTFET2) in the following plots (Figures 6 and 7).

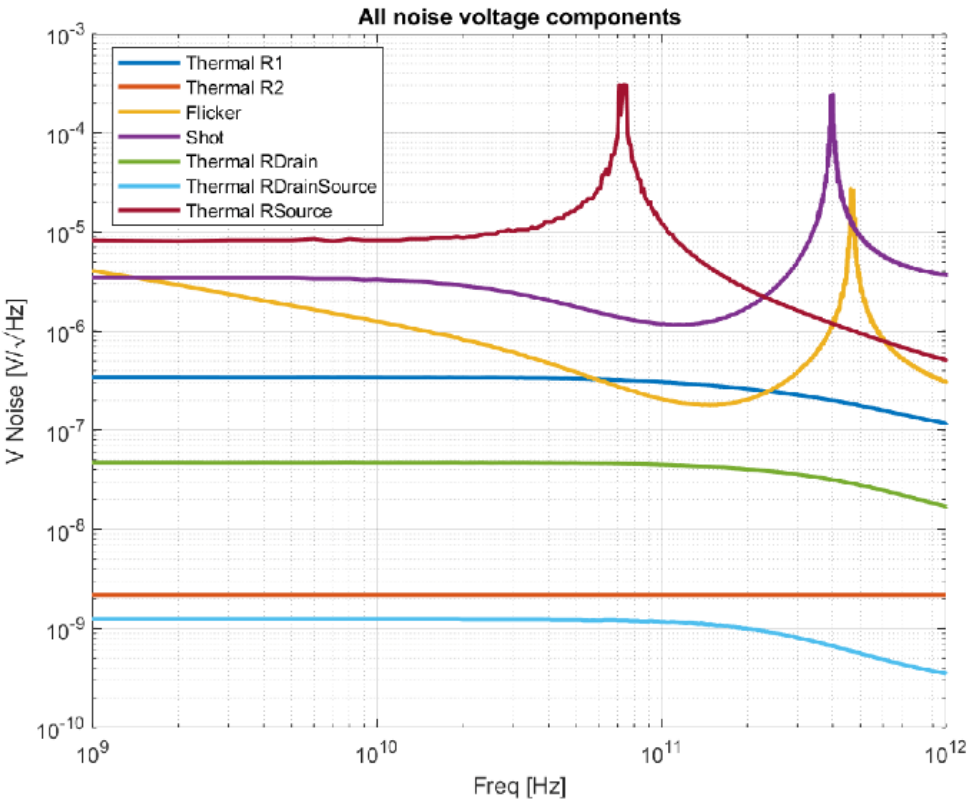

***Figure 6**. Total Noise Voltages [17].*

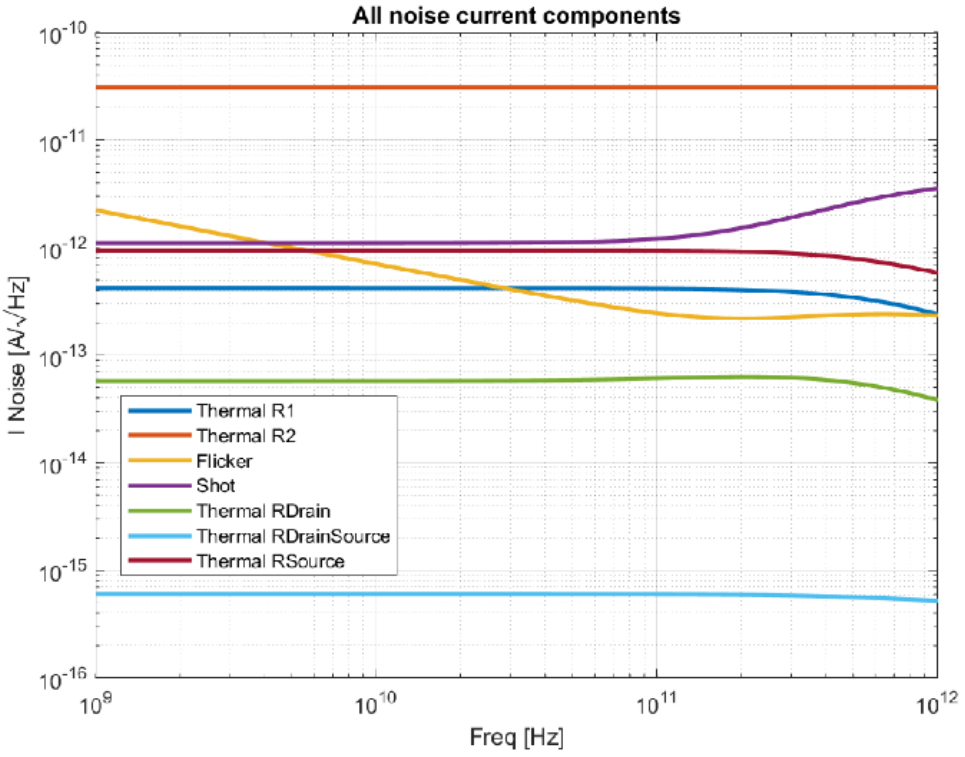

***Figure 7**. Total Noise Currents [17].*

Finally, we considered all noise sources acting together and the results have been plotted in Figures 8 and 9, both taken from our Reference [17].

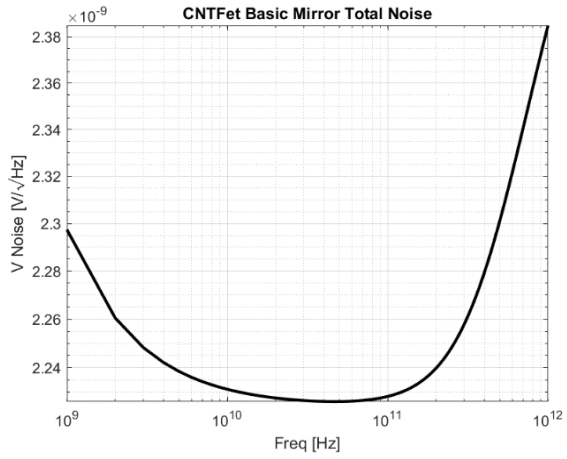

***Figure 8**. CNTFET Mirror V_Total Noise.*

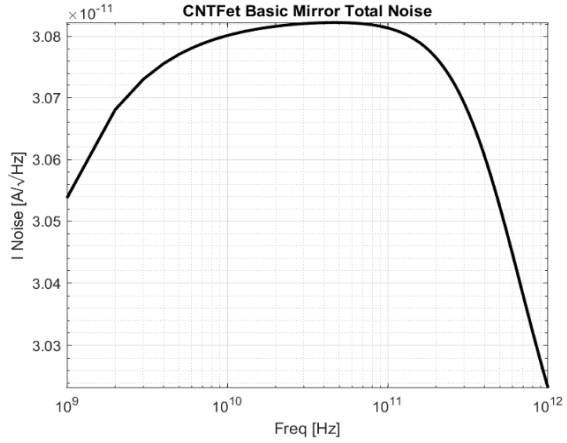

***Figure 9**. CNTFET Mirror I_Total Noise.*

The analysis of Figures 8 and 9 allowed us to say:

1. As expected, flicker and shot noise are very high at low frequency and they decrease while frequency growing;
2. We observe an abnormal behaviour in high frequencies (current or voltage spikes) eventually due to our Thevenin equivalent method used to measure noise in CNTFET Basic-Mirror. Indeed, Thevenin method's expressions for V_N, R_N and I_N lose their efficacy because of phase displacement introduced by parasitic capacities effects in the circuit.

As we have already said, in this paper we want to demonstrate that the same procedure can be also applied to study the noise performance of analog circuits involving MOS devices.

In order to aim this goal, for the MOSFET model, we use the BSIM4 NMOS model, with the same channel length L and width W, equal to 32 nm. of ADS library.

This model can work properly only if its 307 parameters are well set: to do this, we used a design tool available on [25].

The ADS circuits for MOS basic current mirrors used to apply the proposed Thevenin equivalent method, are shown in Figures 10 and 11.

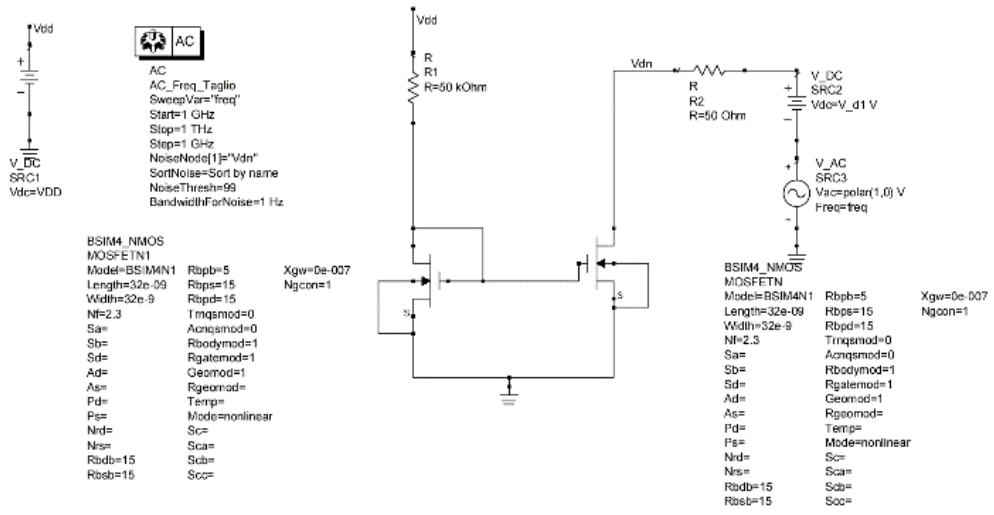

***Figure 10**. MOS Mirror Schematic A.*

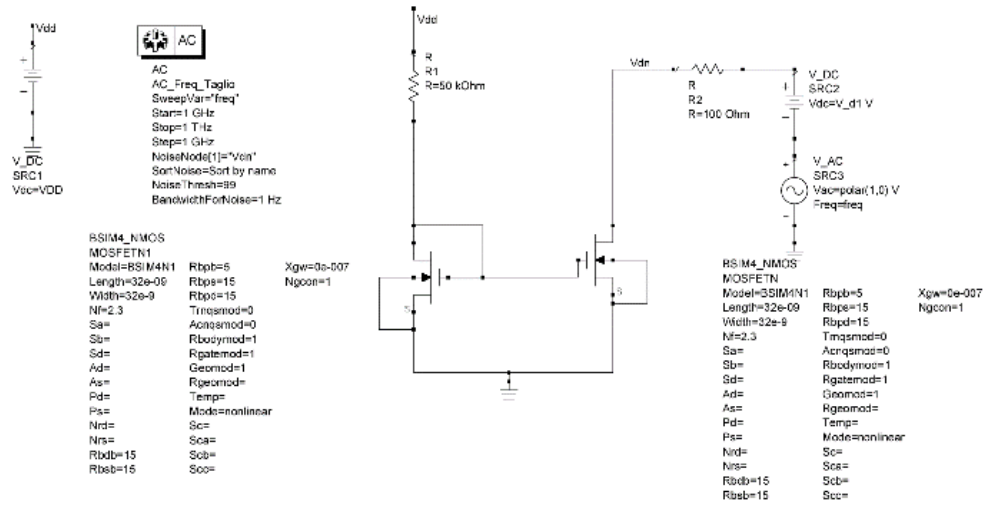

***Figure 11**. MOS Mirror Schematic B.*

Considering all noise sources acting together, the obtained results for MOS devices, have been plotted in Figures 12 and 13.

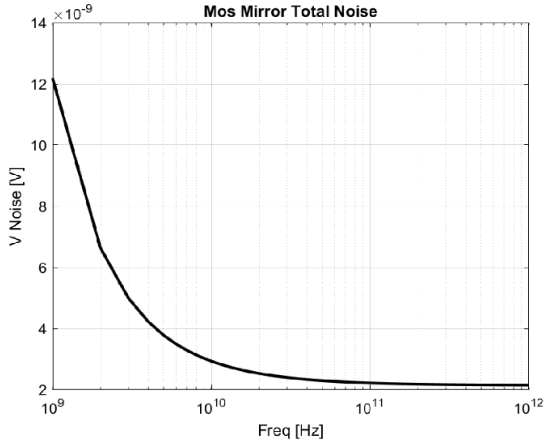

***Figure 12**. MOS Mirror V_Total Noise.*

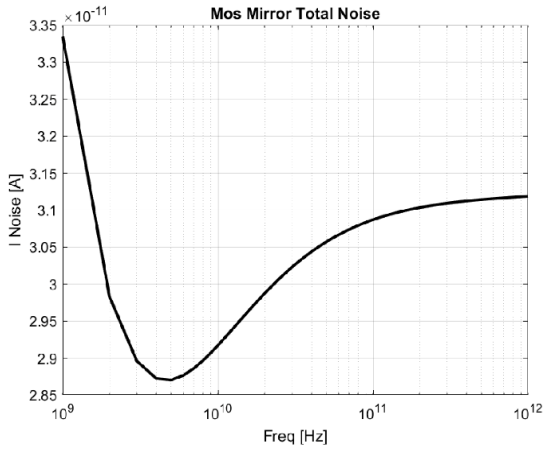

***Figure 13**. MOS Mirror I_Total Noise.*

Moreover, it is possible plotting MOSFET noise total resistance, as shown in Figure 14.

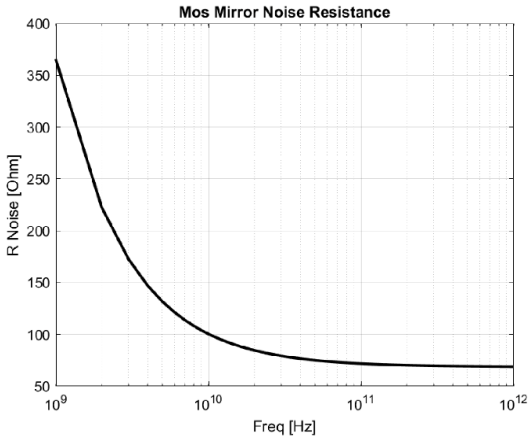

***Figure 14**. Total Noise MOS Mirror Resistance.*

In order to compare the CNTFET and MOSFET mirror performance, in Figures 15, 16 and 17 we plotted total noise components for both devices.

Referring to the previous Figures, we can observe:

1. In low frequency region, total noise voltage produced by MOS basic mirror is higher that then produced by CNTFET basic mirror. As soon as frequency grows both total noise voltages decrease, taking the same trend;

2. For total noise current we notice different trend: at low frequency MOSFet mirror generates high noise which suddenly decreases at its minimum value and then bounces, settling to constant values. CNTFET mirror, instead, produces approximatively a constant total noise current behaviour;
3. About total noise resistance, for CNTFET mirror plot shows a low constant value of about 75 W in all frequency range, while for MOS mirror it follows an inverse trend with frequency.

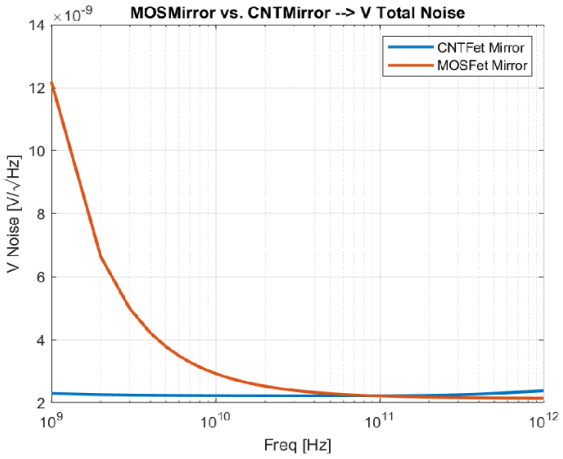

***Figure 15**. V_Total Noise comparison.*

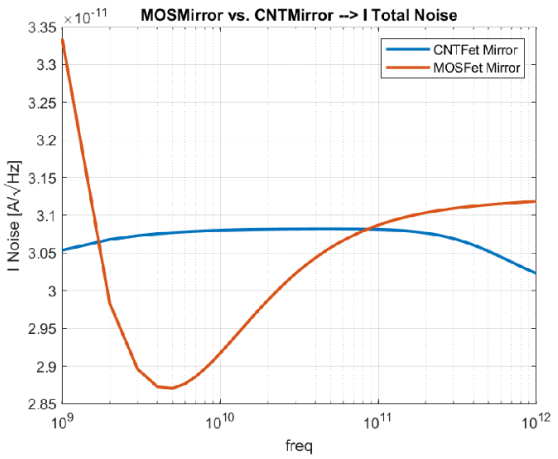

***Figure 16**. I_Total Noise comparison.*

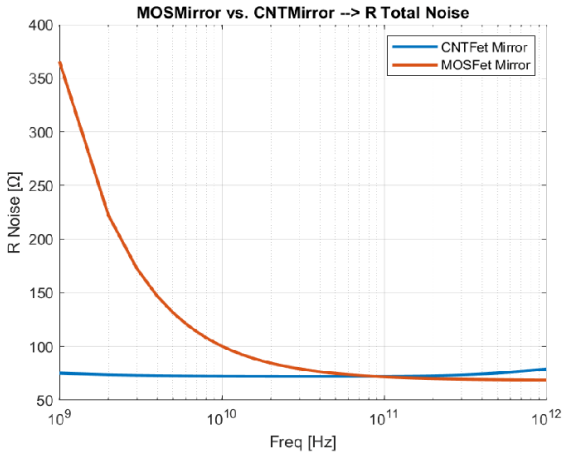

***Figure 17**. R_Total Noise comparison.*

4. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we have presented a procedure, based on Thevenin equivalent method, to analyse the noise effects in analog circuits with CNTFET and MOSFET devices.

In particular we demonstrated that this procedure, already proposed for analog circuits based on CNTFETs [17], can be also applied to study the noise performance of analog circuits involving MOS devices.

As example of analog circuit, we applied the proposed procedure to study a basic current mirror and the simulation results allowed to determine easily the different noise contribution of every single source.

In particular our results shown that the flicker and shot noise are dominant intrinsic noise mechanisms, the first more relevant at lower frequency while shot noise more relevant at higher frequency.

The software used has been Advanced Design System (ADS) which is compatible with the Verilog A programming language.

Currently we are working to study the CNTFETs as memory devices [26-27] and as power amplifier [28], continuing to explore the effects of temperature [29-32] and of noise [33-35] in other circuits based on CNTFETs. Moreover we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [36-37] and

the impact of technology on CNTFET-based circuit's performance [38-39].

We also intend to repeat the proposed simulations using other CNTFET models such the Stanford model [40-43] in order to have comparable results.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. Marani, R., Perri, A. G., "CNTFET Modelling for Electronic Circuit Design", *Electro Chemical Transactions*, 23 (2009) 429 - 437.
2. Gelao, G., Marani, R., Diana, R., Perri, A. G., "A Semi-Empirical SPICE Model for n-type Conventional CNTFETs", *IEEE Transactions on Nanotechnology*, 10 (2011) 506-512.
3. Marani, R., Perri, A. G., "A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software", *Current Nanoscience*, 7 (2011) 245-253.
4. Marani, R., Perri, A. G., "A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications", *International Journal of Electronics*, 99 (2012) 427 - 444.
5. Marani, R., Gelao, G., Perri, A. G., "Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design", *Microelectronics Journal*, 44 (2013) 33-39.
6. Marani, R., Perri, A. G., "Modelling of CNTFETs for Computer Aided Design of A/D Electronic Circuits", *Current Nanoscience*, 10 (2014) 326-333.
7. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis", *Current Nanoscience*, 11 (2015) 515-526.
8. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., "A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part II: Dynamic Analysis", *Current Nanoscience*, 11 (2015) 770-783.
9. Marani, R., Perri, A. G., "Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications", *ECS Journal of Solid State Science and Technology*, 5(2) (2016) M1-M4.
10. Marani, R., Perri, A. G., "A De-Embedding Procedure to Determine the Equivalent Circuit Parameters of RF CNTFETs", *ECS Journal of Solid State Science and Technology*, 5(5) (2016) M31-M34.
11. Marani, R., Perri, A. G., "A Simulation Study of Analogue and Logic Circuits with CNTFETs", *ECS Journal of Solid State Science and Technology*, 5 (2016) M38-M43.
12. Marani, R., Perri, A. G., "A Comparison of CNTFET Models through the Design of a SRAM Cell", *ECS Journal of Solid State Science and Technology*, 5 (2016) M118-M126.
13. Marani, R., Perri, A. G., "Design and Simulation Study of Full Adder Circuit Based on CNTFET and CMOS Technology by ADS", *ECS Journal of Solid State Science and Technology*, 7 (2018) M108-M122.
14. Marani, R., Perri, A. G., "Static Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 121-131.
15. Marani, R., Perri, A. G., "Dynamic Simulation of CNTFET-based Digital Circuits", *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 277-288.
16. Verilog-AMS language reference manual, Version 2.2, (2014).
17. Marani, R., Perri, A. G., "Noise Effects in the Design of Analog Circuits Based on CNTFET", *ECS Journal of Solid State Science and Technology*, 11 (2022) 121010, doi: 10.1149/2162-8777/acad9f.
18. http://bsim.berkeley.edu/models/bsim4/, BSIM Group, Berkeley, University of California, USA, (2020).
19. Marani, R., Gelao, G., Perri, A. G., "A Compact Noise Model for C-CNTFETs", *ECS Journal of Solid State Science and Technology*, 9 (2017) M118-126.
20. Datta S., *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering 3. Electronic Transport in Mesoscopic Systems*, New York: Cambridge University Press, Online ISBN: 978051180577, (1995).
21. Van der Ziel A., *Noise in Solid State Devices and Circuits*, Wiley & Sons, New York, ISBN: 10:0471832340, (1986).
22. Landauer G. M., Gonzalez J. L., "Carbon nanotube FET process variability and noise model for radiofrequency investigations", *Proceedings of 12th IEEE Int. Conference on Nanotechnology (IEEE-NANO)*, (2012), DOI:10.1109/nano.2012.6321963, Birmingham, UK.
23. Landauer G. M., Gonzalez J. L., "A compact noise model for carbon nanotube FETs", *Proceedings of 2012 International Semiconductor Conference Dresden-Grenoble (ISCDG)*, (2012), DOI: 10.1109/ISCDG.2012.6360005.
24. Hooge F. N., "1/f Noise sources", *IEEE Transactions on Electron Devices*, 41 (1994), , 1926-1935, DOI: 10.1109/16.333808.
25. http://ptm.asu.edu/.

26. Marani, R., Perri, A. G., "Study of CNTFETs as Memory Devices", *ECS Journal of Solid State Science and Technology*, 11 (2022), 031001, DOI:10.1149/2162-8777/ ac5846.
27. Marani, R., Perri, A. G., "Review—Design of a Novel Full Adder Circuit based on CNTFET Technology", *ECS Journal of Solid State Science and Technology*, 11 (2022), 051004, DOI:10.1149/2162-8777/ ac6d78.
28. Gelao, G., Marani, R., Perri, A. G., "Study of Power Gain Capability of CNTFET Power Amplifier in THz Frequency Range", *ECS Journal of Solid State Science and Technology*, 11 (2022), 081005, DOI:10.1149/2162-8777/ ac84a7.
29. Marani, R., Perri, A. G., "A Review on the Study of Temperature Effects in the Design of A/D Circuits based on CNTFET", *Current Nanoscience*, 15 (2019), p. 471-480, DOI:10.2174/15734137 14666181009125058.
30. Marani, R., Perri, A. G., "Temperature Dependence of I-V Characteristics in CNTFET Models: A Comparison", *International Journal of Nanoscience and Nanotechnology*, 17(1), (2021), 33-39.
31. Marani, R., Perri, A. G., "Review—Thermal Effects in the Design of CNTFET-Based Digital Circuits", *ECS Journal of Solid State Science and Technology*, 11 (2022), 041006, DOI:10.1149/2162-8777/ ac63e6.
32. Gelao, G., Marani, R., Perri, A. G., "A Formula to Determine Energy Band Gap in Semiconducting Carbon Nanotubes", *ECS Journal of Solid State Science and Technology*, 8 (2019), p. M19-M21, DOI: 10.1149/2.0201902jss.
33. Marani, R., Perri, A. G., "Comparative analysis of noise in current mirror circuits based on CNTFET and MOS Devices", *International Journal of Nanoscience and Nanotechnology*, 17(2), (2021), 121-129.
34. Marani, R., Perri, A. G., "Noise effects in the Design of Digital Circuits Based on CNTFET", *ECS Journal of Solid State Science and Technology*, 11 (2022), 031006, DOI:10.1149/2162-8777/ ac5eb1.
35. Marani, R., Perri, A. G., "Noise Effects in the Design of Analog Circuits Based on CNTFET", *ECS Journal of Solid State Science and Technology*, 11 (2022), 121010, DOI:10.1149/2162-8777/ acad9f.
36. Marani, R., Perri, A. G., "Editors' Choice—Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits", *ECS Journal of Solid State Science and Technology*, 9 (2020), 021004, DOI: 10.1149/2162-8777/ab69b2.
37. Marani, R., Perri, A. G., "A Procedure to Analyze a CNTFET-based NOT gate with Parasitic Elements of Interconnection Lines", *International Journal of Nanoscience and Nanotechnology*, 17(3), (2021), 161-171.
38. Marani, R., Perri, A. G., "Impact of Technology on CNTFET-Based Circuits Performance". *ECS Journal of Solid State Science and Technology*, 9 (2020), 051001 DOI:10.1149/2162-8777/ ab9185.
39. Gelao, G., Marani, R., Perri, A. G., "Analysis of Limits of CNTFET Devices through the Design of a Differential Amplifier", *ECS Journal of Solid State Science and Technology*, 10 (2021), 061009, DOI:10.1149/2162-8777/ ac08df.
40. Deng, J., Wong, H.-S. P., "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region", .*IEEE Transactions on Electron Devices*, 54 (2007) 3186-3194.
41. Deng, J., Wong, H.-S. P., "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking", *IEEE Transactions on Electron Devices*, 54 (2007) 3195-3205.
42. Lee, C-S., Pop, E., Franklin, A.D., Haensch, W., Wong, H.-S. P., "A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nmRegime—Part I: Intrinsic Elements", *IEEE Transactions on Electron Devices*, 62 (2015) 3061-3069.
43. Lee, C-S., Pop, E., Franklin, A. D., Haensch, W., Wong, H.-S. P., "A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nm Regime—Part II:Extrinsic Elements, Performance Assessment,and Design Optimization", *IEEE Transactions on Electron Devices*, 62 (2015) 3070-3078.