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# Study the Effect of Silicon Nanowire Length on Characteristics of Silicon Nanowire Based Solar Cells by Using Impedance Spectroscopy

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***Abstract:***
*Silicon nanowire (SiNW) arrays were produced by electroless method on polycrystalline Si substrate, in HF/ $AgNO_3$ solution. Although the monocrystalline silicon wafer is commonly utilized as a perfect substrate, polycrystalline silicon as a low cost substrate was used in this work for photovoltaic applications. In order to study the influence of etching time (which affects the SiNWs length) on different elements in AC equivalent circuit of the fabricated solar cells, impedance spectroscopy was accomplished for the first time in forward bias direction and under illumination. Measurements indicated a growth of recombination with increase in etching time that may be attributed to enhancement in the number of defects on nanowires surfaces as a result of increase in the length of SiNWs. This trend reduces recombination resistance in device equivalent AC circuit and reduces the efficiency of solar cells. Impedance spectra and fitting curves also showed that the effective carrier lifetime decreases with increase in etching time.*
***Keywords:*** *Silicon, Nanowire length, Electroless Method, Impedance Spectroscopy, Effective Carrier lifetime.*

## 1. INTRODUCTION

Fabrication of solar cells made from one-dimensional nanostructures, has attracted a great deal of interest amongst researchers as cost-effective and highly efficient devices. Their physical properties however, depend on their nanoscale dimensions, and as such, they provide good application potential in third-generation solar cells for which researchers investigate their electrical and optical properties. Among these nanostructures, SiNWs are very attractive due to their electrical and optical properties and the production methods. Synthesis of SiNWs on silicon surface reduces reflection to around 2.5%, so that they can act as antireflection layer in silicon solar cells [1, 2]. DC measurements have been commonly used to investigate the general characteristics of these solar cells, but impedance spectroscopy as an AC technique have not been prevailing and is widely employed for characterization of electrochemical systems such as dye sensitized solar cells [3-6]. Utilization of AC technique (over a broad frequency range from mHz to MHz) beside DC measurements, can provide valuable information about different main processes in solid state solar cells [7]. To study the solar cell AC response, the device should be modeled by an appropriate equivalent circuit that includes all the physical mechanisms in device configuration like depletion layer capacitance $C_j$

(junction capacitance) and the excess minority carriers capacitance $C_d$ (diffusion capacitance). The impedance of this circuit may be written as:

$$Z = Z_1 + iZ_2 \quad (1)$$

$$Z_1 = R_S + \frac{R_{sh}}{1+R_{sh}^2 C_j^2 \omega^2} + \frac{R_r}{1+R_r^2 C_d^2 \omega^2} \quad (2)$$

$$Z_2 = -\frac{R_{sh}^2 C_j \omega}{1+R_{sh}^2 C_j^2 \omega^2} - \frac{R_r^2 C_d \omega}{1+R_r^2 C_d^2 \omega^2} \quad (3)$$

Where $Z_1$ and $Z_2$ are the real and imaginary parts of circuit impedance, respectively [8]. In this model, resistive outcomes arise from the contact effect (a series resistance $R_S$), shunt resistance (a parallel resistance $R_{sh}$) and the minority carrier recombination ($R_r$) [8-12] as are shown in the equivalent circuit in Figure 1.

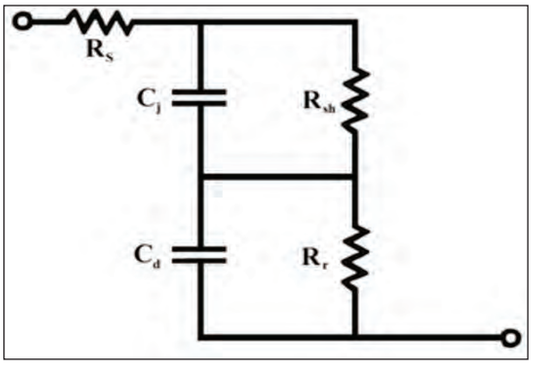


***Figure 1:*** *AC equivalent circuit for the fabricated silicon nanowire based solar cells.*

By analysis of impedance spectra of solar cells in different bias conditions, one can determine some important parameters like effective carrier lifetime. In this work, electroless method, was utilized as a simple and low-cost technique to produce SiNWs on polycrystalline silicon substrate and impedance spectra of the fabricated SiNWs solar cells was investigated for the first time in the forward bias direction ($V=V_{OC}$), and under illumination. Under this condition, the diffusion capacitance rises because of minority carrier accumulation and determines the capacitance response of the device.

## 2. EXPERIMENTAL

P-type polycrystalline Si wafer with resistivity around 30-40 Ω cm from Bayer was employed as substrate. The silicon samples were cut into 1×1 $cm^2$ and then tube diffusion method was utilized to construct n-p-n junctions in Si wafer. Diffusion process was carried out by means of $POCl_3$ as phosphorus source at 900˚C for 60 min in nitrogen atmosphere. Rear emitter was removed from the back surface of diffused wafer by HF, $H_2SO_4$, $HNO_3$, and $H_2O$ solutions.

Afterwards different pollutions were removed from the substrate with immersing the Si wafer in acetone, ethanol, HF (5 M) and DI water for 10 min each. Electroless process was performed in a sealed teflon vessel by immersing Si wafer in HF (5 M) and $AgNO_3$ (0.02 M) solutions to produce SiNWs on the front surface of the substrates. Experiments were conducted for 30 min at different reaction temperatures of 40, 45, 50, 55, 60, and 65˚C for obtaining the optimum etching temperature. Results show that increase in temperature up to 55˚C, improves nucleation and single SiNWs are formed on substrate around 50˚C and 55˚C, while with further rise in temperature, nucleation seems to decrease and belt-like connections are observed amongst SiNWs at 65˚C.

Therefore, 55˚C was considered as the optimum temperature for synthesis of SiNWs. In order to study the effect of reaction time on different photovoltaic parameters, four samples were prepared at 55˚C using different reaction times from 30 min to 60 min. To investigate the SiNWs morphology, FESEM (Hitachi S-4160) images were employed. To collect photo generated carriers, 100 nm Al and 100 nm ITO were deposited on samples surfaces by thermal evaporation and sputtering methods as rear and front electrodes, respectively. Figure 2, illustrates the schematic view of the solar cell structure in this work.

The photovoltaic measurements were performed by solar simulator (Luzchem) and IVIUMSTAT (IVIUM) under AM1.5 condition. Impedance spectroscopy was fulfilled in forward bias condition ($V=V_{OC}$) under illumination (AM1.5)


***Figure 2:*** *Schematic view of the solar cell structure.*

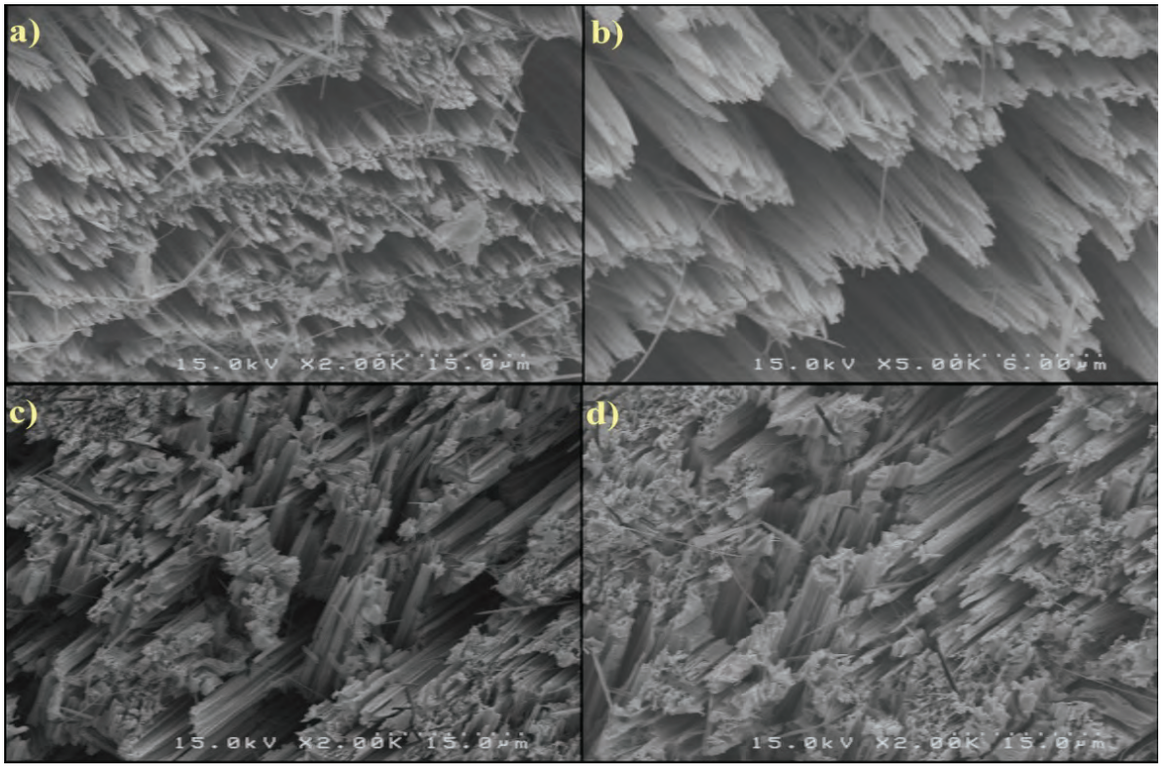


***Figure 3:*** *FESEM images from different parts of the etched silicon wafer, (a) and (b) SiNWs, and (c) and (d) formless structure with high porosity.*

and in frequency range from 500 KHz to 1 Hz with oscillating amplitude around 10 mV in order to maintain the linearity of response.

## 3. RESULTS AND DISCUSSIONS

Silicon wafer crystalline direction is a consequential factor in electroless method which controls the SiNWs growth direction on silicon wafer. In this technique, desired direction for growth of SiNWs can be achieved by selecting a special monocrystalline silicon wafer. Due to this fact, employing polycrystalline silicon wafer as a raw wafer causes the growth of Si nanostructures in different directions on the silicon surface. The reaction time has important role on SiNWs length, but short etching times prevent all parts of the surface to be etched uniformly, so 30 min and 60 min were selected as minimum and maximum times for the reaction. Moreover the main focus was to attain an insight on the effect of etching time (nanowire length) on AC equivalent circuit elements of solar cells. As is evident in Figure 3, FESEM images show disparate Si nanostructures on different parts of silicon wafer, which reveals that SiNWs growth direction is strongly dependent on wafer crystallinity.

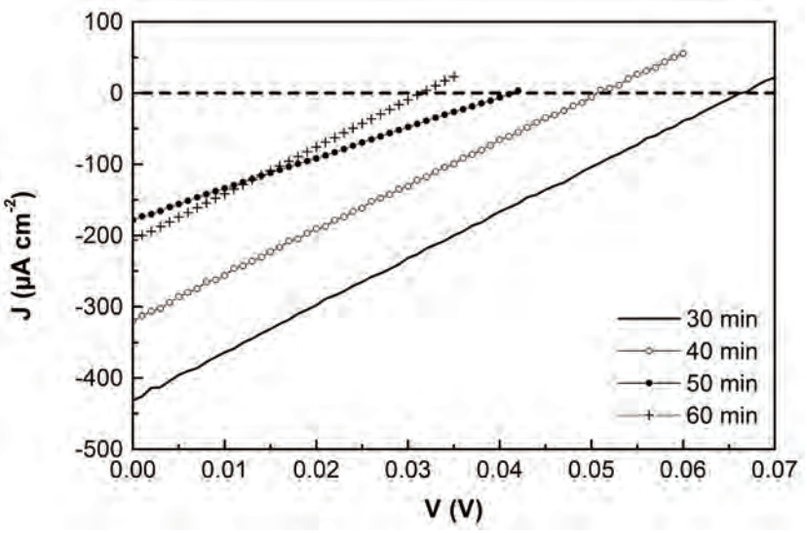


***Figure 4:*** *IV diagram of solar cells for different etching times.*

Synthesis of these nanostructures reduces the reflection and increases the light absorption by solar cells surfaces. This behavior is because of optical antenna effect and severe light trapping by multiple scattering of the incident light among SiNWs. It was found in this study that the etching time just controls the length of SiNWs, and there is a near linear relationship between SiNWs length and the reaction time, while SiNWs length is independent of the reaction temperature. To study the effects of SiNWs lengths on different photovoltaic responses of solar cells, four samples were produced using different etching times and then DC photovoltaic measurements were accomplished under AM1.5 conditions. I-V diagrams of these cells are shown in Figure 4.

The efficiency can be calculated from:

$$\eta_{AM1.5}\% = \frac{P_m}{P_L} \times 100 = \frac{I_m.V_m}{P_L} \times 100 = \frac{I_{SC}.V_{OC}.FF}{P_L} \times 100 \quad (4)$$

$$FF\ \% = \frac{I_m.V_m}{I_{sc}.V_{oc}} \times 100 FF\ \% = \frac{I_m.V_m}{I_{sc}.V_{oc}} \times 100 \quad (5)$$

where $P_m$=$I_m$.$V_m$ is the maximum power output of solar cells ($I_m$ and $V_m$ correspond to current and voltage at the point of maximum power), $P_L$ is the power of incident light, *FF* is the fill factor of solar cell in %, $J_{SC}$ and $V_{OC}$ are short circuit current density (in mA.cm$^{-2}$) and open circuit voltage (in V) of the solar cell, respectively. It is suggested, that low *FF* experienced here could be attributed

***Table 1:*** *DC parameters of solar cells fabricated using different etching time.*

| Etching time (min) | η (%) | $V_{OC}$ (V) | $J_{SC}$ (μA/cm$^2$) | FF (%) |
|---|---|---|---|---|
| 30 | 7.04E-03 | 0.066 | 431` | 25 |
| 40 | 4.04E-03 | 0.051 | 319 | 25 |
| 50 | 1.84E-03 | 0.041 | 178 | 25 |
| 60 | 1.64E-03 | 0.031 | 207 | 26 |

to poorly qualified junction formed between front electrode and SiNWs, which causes large quantities of Rs for all samples (Table 2). Meanwhile with increasing the etching time, other parameters such as efficiency, open circuit voltage and short circuit current density were decreased which is evident in Table 1.

These reductions may be attributed to increase of SiNWs surfaces, which bring about numerous recombination centers for light generated carriers. In other words, the short SiNWs can drastically trap the incident light such that with increase in etching time, the relative decrease of reflection rate from the surface is small, while the recombination rate of charge carriers considerably increases with overall diminish of solar cells efficiency.

In forward direction biasing and operating under illumination, the dynamic response of device is strongly dependent on recombination mechanisms and charge accumulation. By applying the bias voltage (equals to $V_{OC}$) and under illumination, a uniform distribution of excess carriers yields because DC current is not permitted.

So, the solar cell can operate in high-injection conditions. These excess electrons and holes in conduction and valance bands cause separation of $E_{Fn}$ and $E_{Fp}$ and create a voltage. In this circumstance, diffusion capacitance increases and overcomes the junction capacitance ($C_d > C_j$).

These carriers have two ways to leak out: either through the external pathway or through the recombination resistance. AC equivalent circuit of solar cell should include all of these parameters. The experimental values of the impedance spectra at forward bias and under illumination are shown in Figure 5.

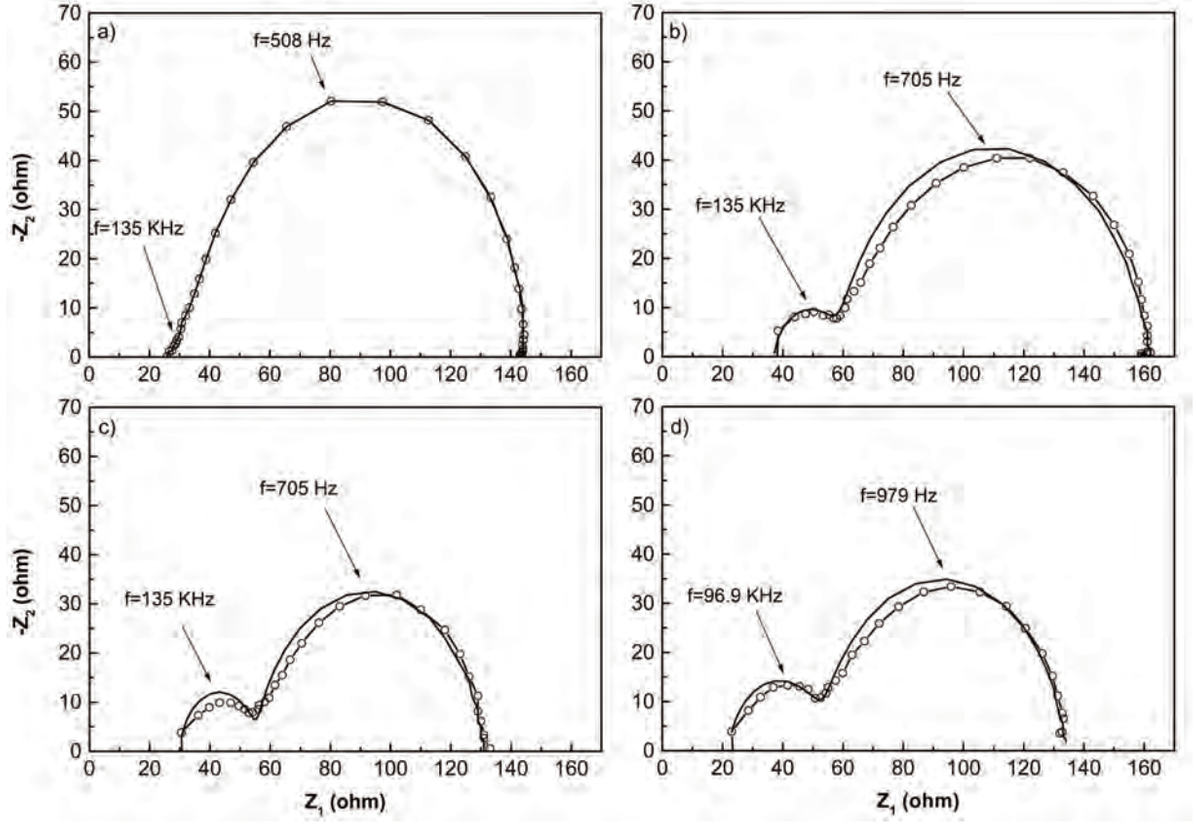


***Figure 5:*** *Impedance spectra of SiNWs solar cells for different etching times containing experimental (black circles) and fitting values (blue squares).*

***Table 2:*** *Parameters of AC equivalent circuit for solar cells prepared using different etching time.*

| Etching time (min) | $R_S$ (Ohm) | $R_{sh}$ (Ohm) | $C_j$ (F) | $R_r$ (Ohm) | $C_d$ (F) |
|---|---|---|---|---|---|
| 30 | 26.5 | 10.5 | 1.4E-06 | 144 | 5.56E-06 |
| 40 | 37 | 21 | 4.0E-07 | 104 | 6.50E-06 |
| 50 | 30 | 25 | 1.0E-07 | 76 | 6.45E-06 |
| 60 | 22 | 31 | 7.0E-08 | 81 | 3.20E-06 |

According to this Figure, impedance spectra for all samples have two semicircles in Nyquist plot that come from a double RC subcircuits in AC equivalent circuit of solar cells. Larger semicircle comes from junction capacitance and shunt resistance, and smaller semicircle appears from diffusion capacitance and recombination resistance, and its shape depends on the etching time. Frequency is shown as extra information at each extremum, and it is not used in calculation of lifetimes. Fitting process was carried out by IVIUMSTAT (IVIUM) program (which supports ZView software) with double RC subcircuits in parallel, in connection with $R_S$ in series (Figure 1). The values of all parameters obtained from the fitting procedure are depicted in Table 2.

According to this table, with increasing the etching time (increase in SiNWs length), recombination resistance decreases and this trend is more efficient than the growth of shunt resistance. Application of SiNWs as a light trapping active region in the fabricated solar cell, increases the surface to volume ratio of the silicon structure, which in turn highlights the influence of surface defects acting as recombination sites. In other words, the carrier recombination depends strongly on the quasi levels on the SiNWs surface. An increase in the etching time causes the silicon nanowires lengths to increase, so dangling states on silicon wafer move up and $R_r$ reduces. It is proposed that this factor is responsible for decrease in solar cells efficiency with increase in etching time. To investigation the effect of SiNWs length on effective carrier lifetime ($\tau_{eff}$), fitting parameters and following equation were used:

$$\tau_{eff} = R_r C_d \quad (6)$$

As indicated in Figure 6, by increasing the etching time, effective carrier's lifetime decreases.

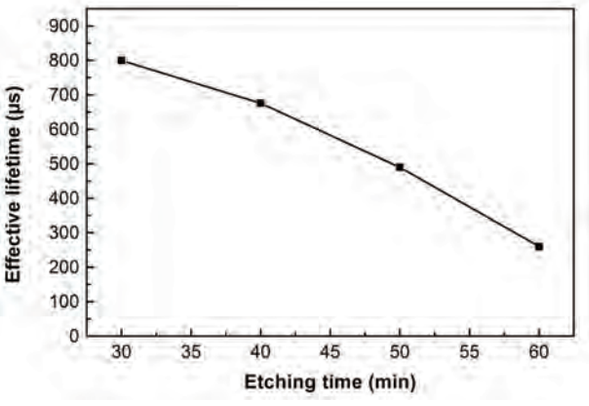


***Figure 6:*** *Effective carrier lifetime versus etching time.*

This trend is due to rising of nanostructures surfaces and reduction of recombination resistance. The effects of employing monocrystalline silicon as substrate and passivation process on impedance spectra of SiNWs solar cells are under consideration.

## 4. CONCLUSION

In this work SiNWs have been synthesized by electroless technique on polycrystalline silicon wafer and the influence of SiNWs lengths on DC and AC response of solar cells were studied. To obtain device response at high injection conditions, impedance spectroscopy was accomplished in forward bias condition ($V=V_{OC}$) under illumination (AM1.5) and in frequency range from 500 KHz to 1 Hz with oscillating amplitude around 10 mV. Impedance spectra show two semicircles at Nyquist

plot that can be attributed to two RC subcircuits in solar cell AC equivalent circuit. Measurements indicated that the efficiency of solar cells decreases with increase in etching time and AC fitted parameters showed reduction in recombination resistance for longer etching times. This behavior originates from increased nanostructures surfaces that decline the effective carrier lifetime. Using monocrystalline silicon as substrate and passivation process may improve the photovoltaic characteristics.

## ACKNOWLEDGEMENT

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