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Analysis of Temperature Effects in the Design of NOT Gate Based on CNTFET

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Abstract

This paper presents a procedure to analyze the effects of temperature in CNTFET-based NOT gate using a compact semi-empirical model, already proposed by us. The proposed analysis allows to determine the noise margin and static power in different voltage supplies and temperature conditions. In particular the noise margin decreases and static power increases with temperature, so it can be asserted that low temperature is the most advantageous condition. This is true except for the case 100 K - 200 mV where noise margin is much lower than the expected value due to the double peak in gain function. In terms of power, it should be also noted that decreasing temperature from 200 K to 100 K does not produce any remarkable result. The proposed procedure can be applied to analyze the effects of temperature in the design of A/D circuits based on CNTFET.

Keywords: *CNTFET, Modelling, Temperature Effects, NOT gate, Verilog-A, Computer Aided Design (CAD).*

1. INRODUCTION

For a wide range of technological applications, the need to reduce electronic devices dimensions is emerging, leading the effort of researchers into the scaling of electronic elemental cell. The state of the art is 12 nm MOSFET based electronics for digital applications and a further decrease of the scaling ratio is challenged by the impossibility of handle quantum phenomena, like tunnel effects [1-2]. Dimensions near the semiconductors reticular constants produces overheating and high malfunction probability.

One of the solution to the problem was found in the Carbon NanoTubes (CNTs). The purpose was to build MOS-like devices in order to use the advanced knowledge acquired instead of resetting completely the know-how.

As it is known, the Carbon NanoTubes [1-2] consist in a hexagonal mesh of carbon atoms wrapped in cylinder shapes, some time with closing hemispherical meshes on the tips. These tubes could have various radii, lower than two nanometers and, since they could be extended several millimeters, they have a huge length/diameter ratio making them unidimensional structures. Depending on the mesh torsion, denoted as *chirality*, electronic band structure of CNT changes, band gap may appear making them semiconductors, or may not appear, making them conductors [1-3].

A CNTFET is a Field Effect Transistor that has the typical structure of the MOSFET, but uses a single or multiple CNTs instead of silicon as a channel material. CNTFETs are made with extended and highly doped drain/source regions which give them MOSFET-like performances.

In literature various CNTFETs models, used in the design of electronic circuits, have been proposed. In [4-11] we have already proposed a compact, semi-

empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A [12].

In [13] we have already review a method to analyse the effects of temperature in the design of a harmonic oscillator and an OTA, examining at first the impact of temperature variations in the CNTFET output and trans-characteristics, the output resistance and the transconductance.

In this paper, in order to prove that the procedure proposed in [13] can easily be applied to any other circuit based on CNTFET, we analyse the effects of temperature variations in the design of a NOT gate, using our CNTFET model.

The presentation is organized as follows. Section 2 gives a brief description of our model, with reference to Equations on which the CNTFET model is based.

The discussion of obtained results, together with the description of the setup-work used during the simulations, is given in Section 3. The conclusions and future developments are given in Section 4.

2. A BRIEF REVIEW OF OUR CNTFET MODEL

2.a I-V Model

An exhaustive description of our CNTFET model is in our Refs [4-5] and therefore the reader is requested to consult them. In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [14], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT}, have the expressions reported in [4-6]. In the simulations, shown in Section 3, our model has been translated in the programming language Verilog-A and then implemented on the simulator Advanced Design System (ADS).

2.b C-V Model

An exhaustive description of our C-V model is widely described in our References [6-11] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behavior, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances, achieving this goal using an empirical method [15], exhaustively described in [4-5].

In this way all elements of the equivalent circuit of Figure 1 can be determined.

It is similar to a common MOSFET one [15] and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

3. NOT GATE DESIGN

Referring to an inverter, for a static analysis we can determine the voltage transfer characteristic, VTC (Figure 2), and then the noise margins, which provide a measure of the maximum external voltage noise that can be overlapped to the input signals, without causing unwanted output variation.

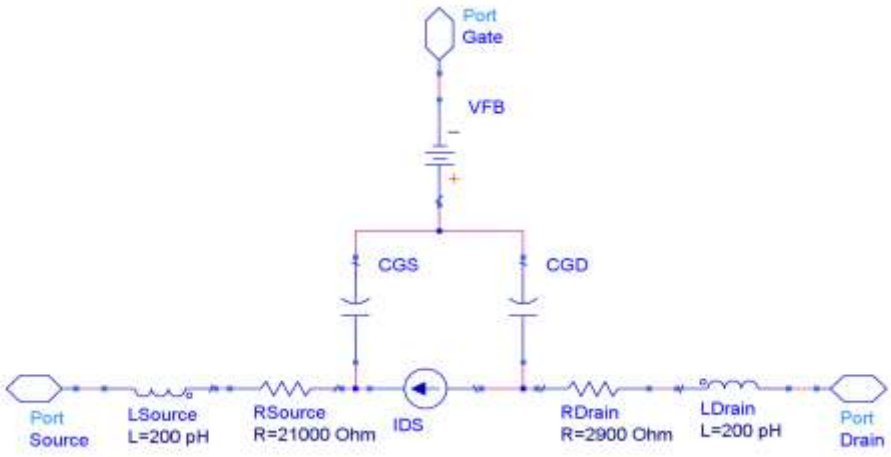

Figure 1. *Equivalent circuit of a n-type CNTFET.*

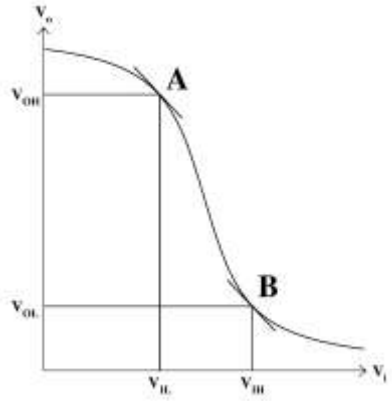

Figure 2. *Voltage transfer characteristic for an inverter.*

The noise margins, whose values are necessary in the design of digital circuits, are determined from the -1 slope points on the VTC, indicated by the letters A and B in Figure 2, which delimit the amplification range of the device. V_{OH} and V_{IL} (point A), represent respectively the valid minimum output voltage at high level and the valid maximum input voltage at low level. Similarly V_{OL} and V_{IH} (point B) the valid maximum output voltage at low level and the valid minimum input voltage at high level.

The noise margins are defined as follows [16-17]:

$NM_H = V_{OH} - V_{IH}$ for high voltage

and

$NM_L = V_{IL} - V_{OL}$ for low voltage.

When the input voltage V_I is between V_{IL} and V_{IH}, the logic gate is in an undefined state, which is an operative condition that we must avoid to make sure the logic levels are within well-defined regions.

Moreover, in the following simulations we choose n-type and p-type parameters to be complementary in order to realize a symmetric behavior when possible. We also used dual voltage supply to obtain a better view of VTC.

Static power (P_S) is the power dissipated by the logic gate when the input is fixed on '0' or '1' level. As plausible voltage values for high and low input, V_{OH} and V_{OL} were chosen, considering the logic gate to be driven by another of the same type.

In [16-17], to verify the validity of the obtained results at 300 K, they have been compared with those of Wong model [18-19], resulting in good agreement. Therefore the reader is requested to consult our References [16-17].

However our model allows significant improvements compared to Wong model, because we have obtained a lighter ensuring compile and shorter execution time, without losing in accuracy, which are the main characteristics to obtain an easy implementation in circuit simulators.

Before examining the thermal effects, a preliminary analysis was conducted about the voltage supply dependency for three selected temperature values. It was observed that in low temperature

conditions, too low voltage supply brings to not acceptable operation, because the VTC gain is lesser than 0. This can bring to an undetermined condition in presence of noise. Then we choose two voltage supplies that can work properly and examine the temperature dependence for a wider set of values.

The circuit used to simulate a NOT logic gate consists in two CNTFETs configured as shown in Figure 3, while the set up to determine gain, noise margin and static power is shown in Figure 4.

Gain is evaluated as:

$$G=\frac{V_{O1}-V_{O2}}{dV}$$

where dV is set to 0.001 V.

First, we set a parametric sweep on the V_{DD}, from 150 mV to 300 mV with 25 mV step, to evaluate the influence of voltage supply. We repeated the simulations for 100 K, 300 K and 500 K.

Figures from 5 to 13 show the trends of V_{out}, of gain and of power as a function of V_{in}.

It can be also noticed that the diagram of power for 100 K temperature is again different: instead of decreasing exponentially for each voltage value, it fast decreases near zero and then continues nearly flat until V_{DD}. It should be noted that the graph is in logarithmic scale on the y axis.

It is also important to observe that each diagram is perfectly symmetrical, thanks to the complementarity of the devices used and to the symmetrical operation of the NOT gate. This cannot be guaranteed for the other logic gates.

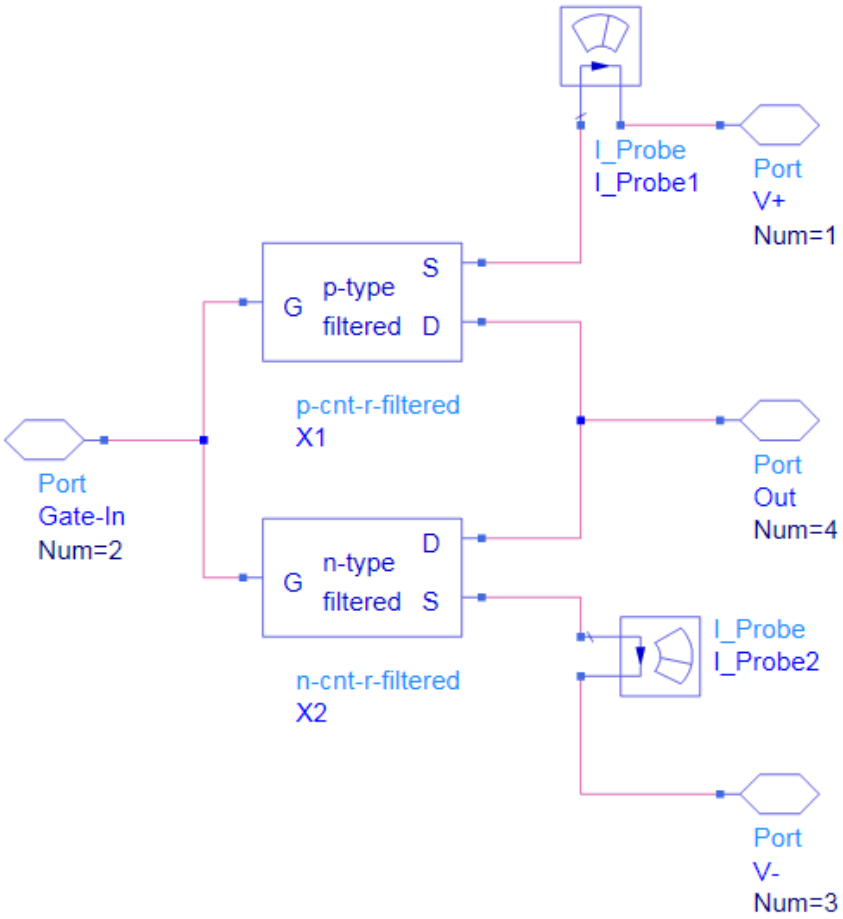

Figure 3. *Circuit used to simulate a NOT logic gate.*

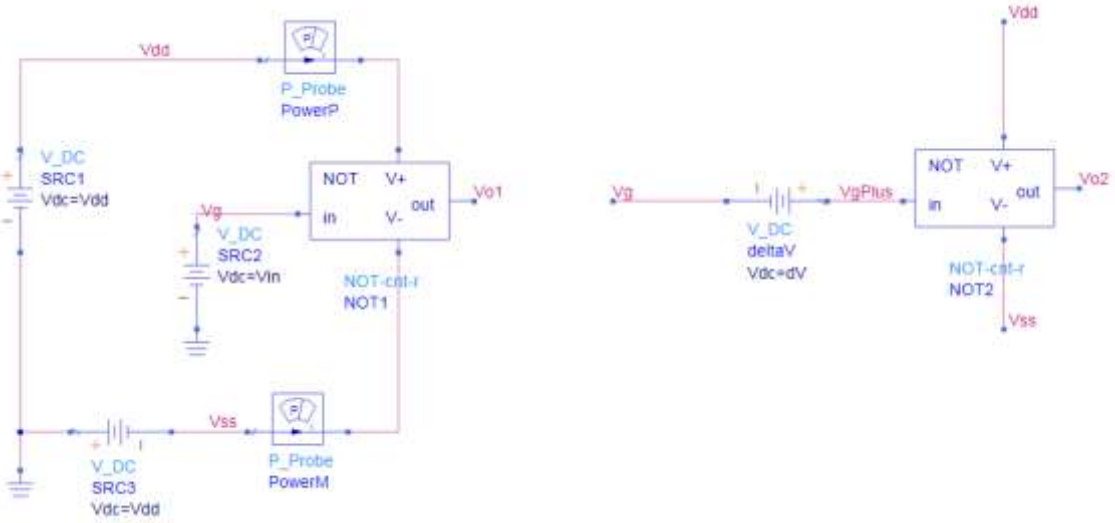

Figure 4. *Set-up to measure gain, noise margin and static power.*

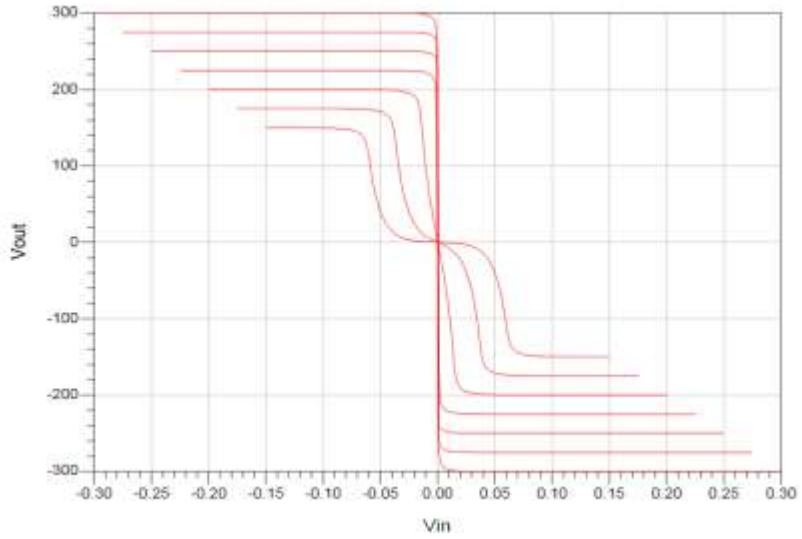

Figure 5. *VTC at 100 K.*

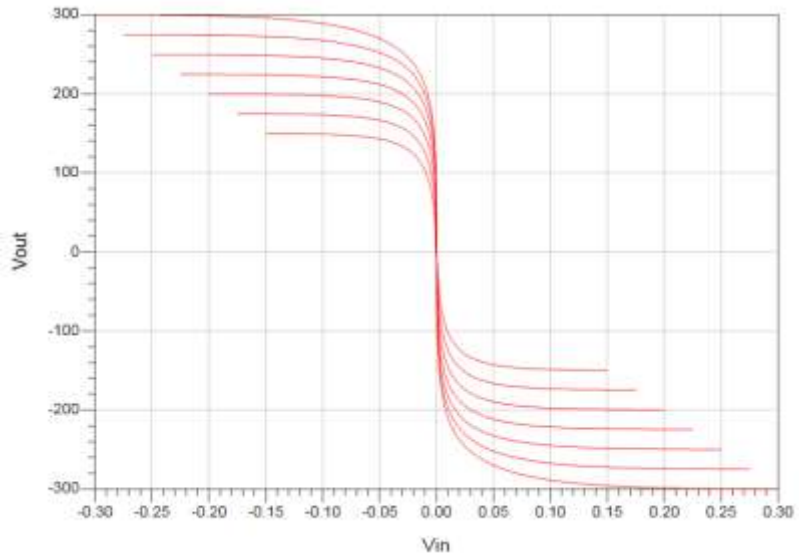

Figure 6. *VTC at 300 K.*

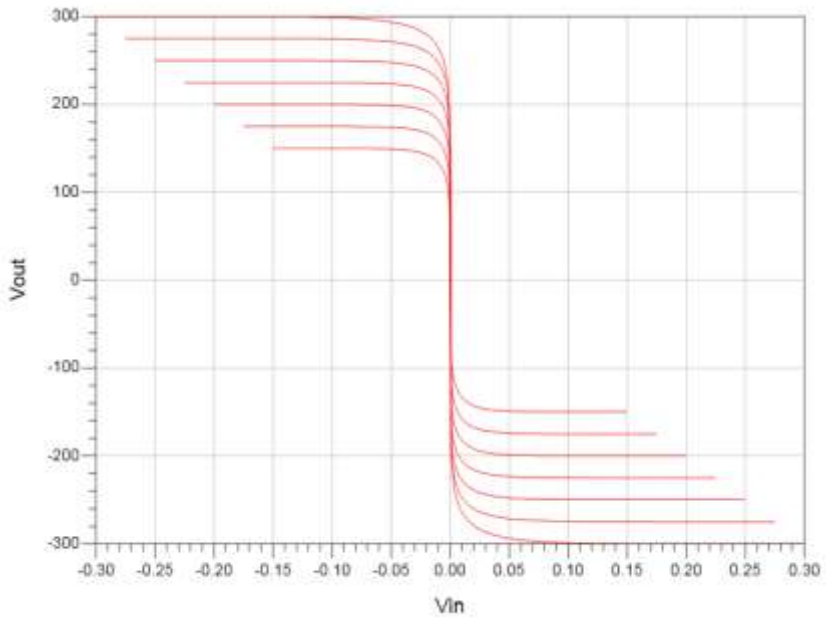

Figure 7. *VTC at 500 K.*

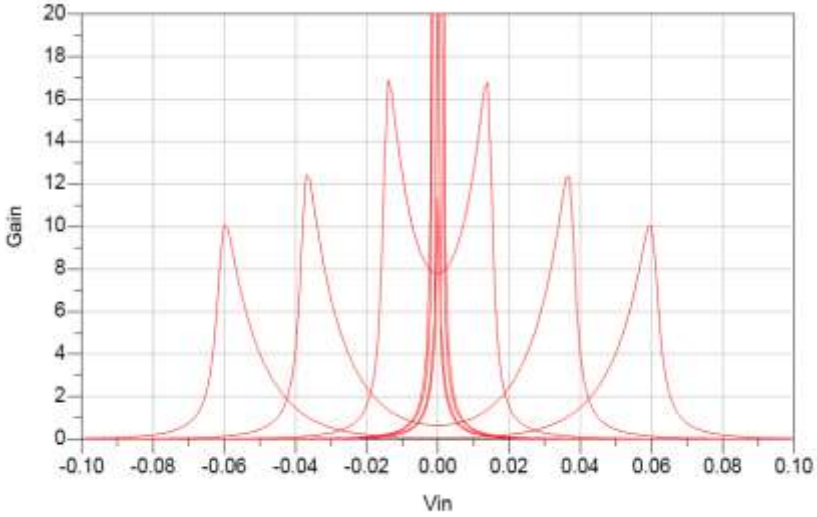

Figure 8*. Gain at 100 K.*

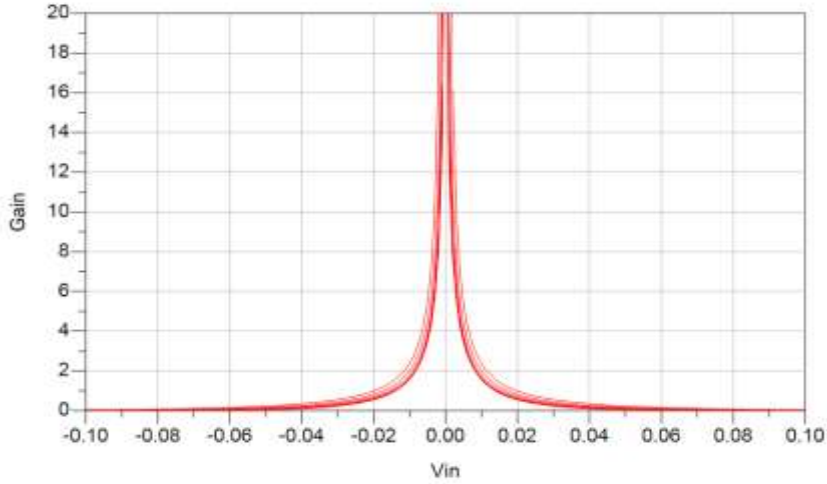

Figure 9*. Gain at 300 K.*

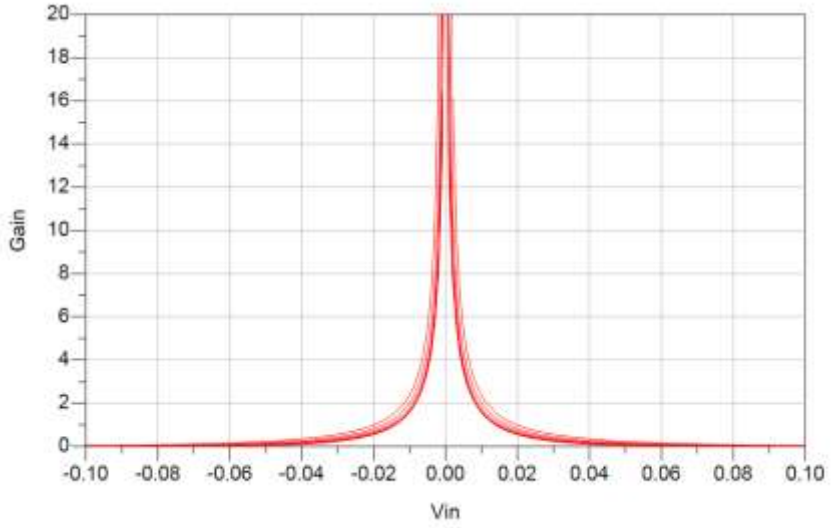

Figure 10. *Gain at 500 K.*

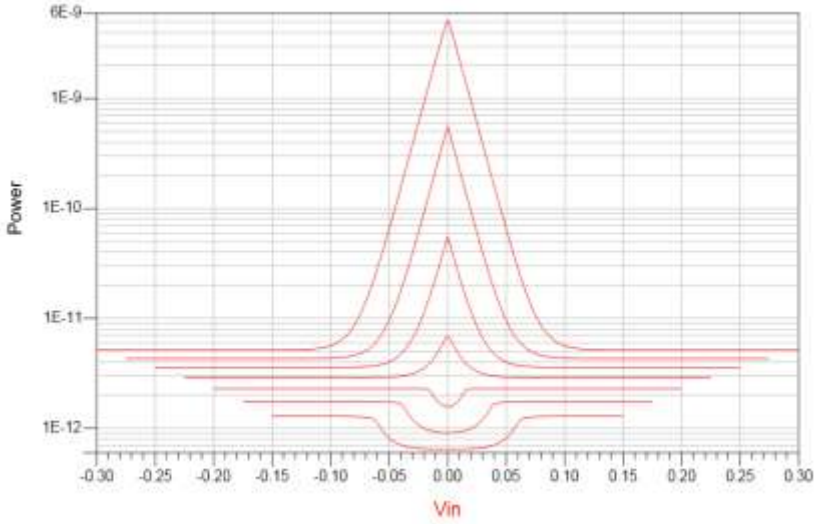

Figure 11. *Static power at 100 K.*

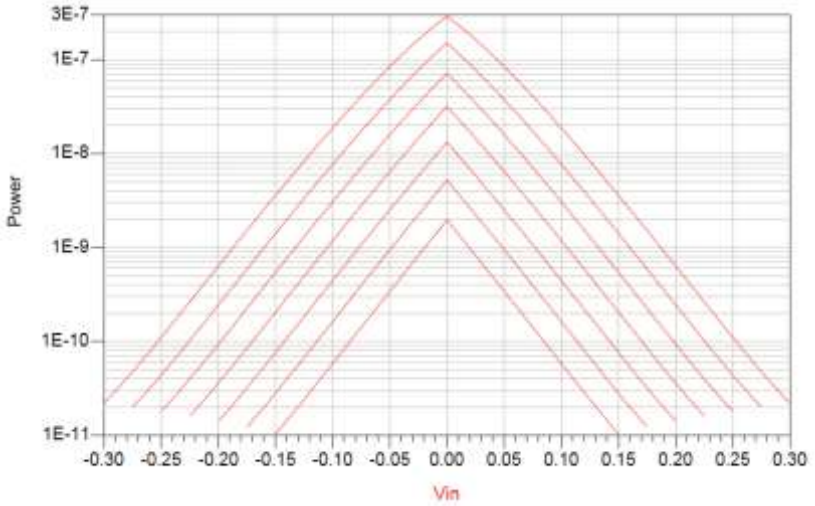

Figure 12. *Static power at 300 K.*

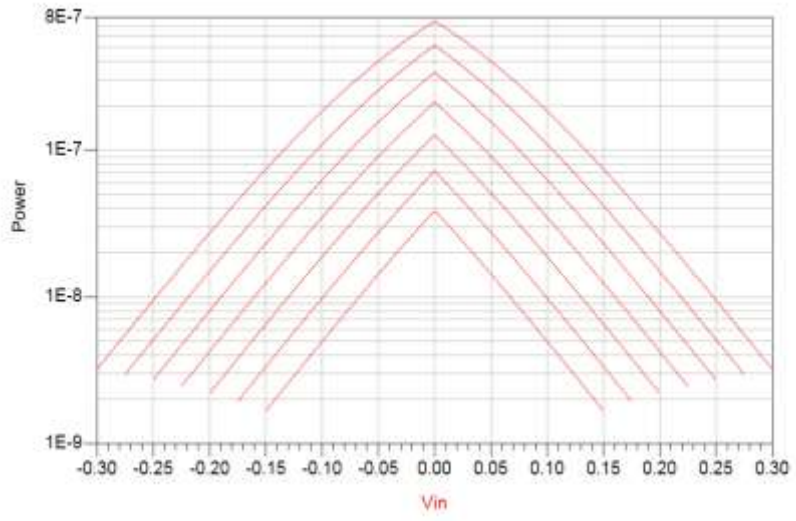

***Figure 13**. Static power at 500 K.*

In Tables 1, 2 and 3 we report the obtained quantities. Points in which the gain G is equal to 1 were obtained from the minimums of the function: |G-1|**.**

***Table 1**.Obtained values at 100 K.*

NOT CNTFET T = 100 K				
V_{DD} (mV)	V_{IH} (mV)	V_{OH} (mV)	NM (mV)	P_S (W)
150				
175				
200	22	193	171	2,3E-12
225	7	220	213	2,9E-12
250	4	245	241	3,6E-12
275	5	271	266	4,3E-12
300	6	295	289	5,1E-12

***Table 2**. Obtained values at 300 K.*

NOT CNTFET T = 300 K				
V_{DD} (mV)	V_{IH} (mV)	V_{OH} (mV)	NM (mV)	P_S (W)
150	14	138	124	1,5E-11
175	14	163	149	1,8E-11
200	14	187	173	2,1E-11
225	15	212	197	2,4E-11
250	16	235	219	2,9E-11
275	17	257	240	3,5E-11
300	20	279	259	4,2E-11

***Table 3**. Obtained values at 500 K.*

NOT CNTFET T = 500 K				
V_{DD} (mV)	V_{IH} (mV)	V_{OH} (mV)	NM (mV)	P_S (W)
150	25	129	104	2,6E-09
175	25	152	127	3,2E-09
200	26	175	149	3,8E-09
225	27	197	170	4,5E-09
250	29	218	189	5,4E-09
275	32	239	207	6,5E-09
300	35	258	223	8,0E-09

After this preliminary analysis to determine the optimal voltage supply, we continued performing a parametric sweep over temperature from 100 K to 500 K, with 100 K step, considering both cases 200 mV and 300 mV voltage supply.

The obtained results regards to the noise margin and the static power are shown in Figures 14 and 15 respectively.

From obtained results, we can observe that for a fixed temperature value the dependency versus voltage supply is linear for noise margin and exponential for static power. Both increase with voltage as predictable.

Considering the graphs for a fixed voltage supply, we can observe again a linear and exponential dependency versus temperature for noise margin and static power respectively. At the same temperature, both are greater for V_{DD} equal to 300 mV.

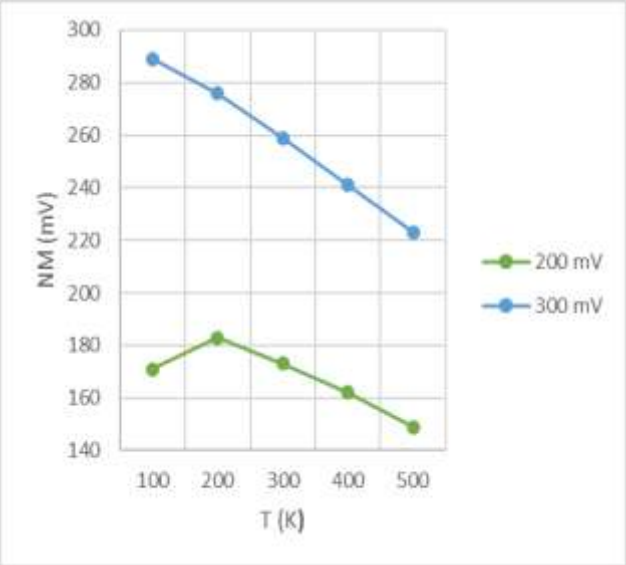

***Figure 14.** Noise margin vs temperature for V_{DD} 200 mV and 300 mV.*

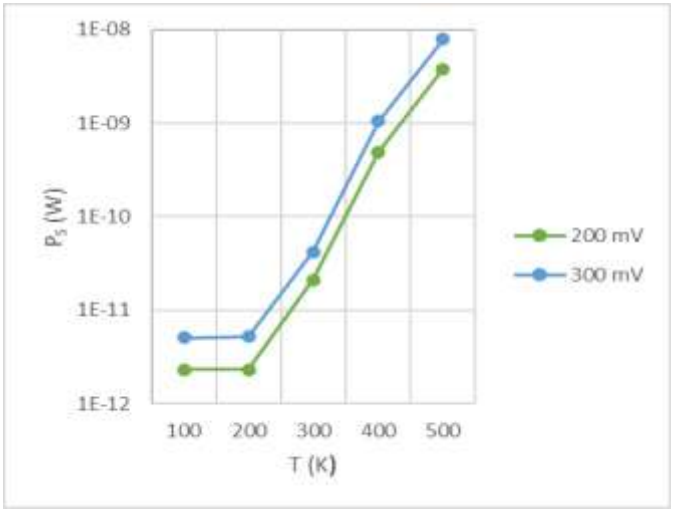

***Figure 15**. Static power vs temperature for V_{DD} 200 mV and 300 mV.*

4. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we presented a procedure to analyse the effects of temperature in CNTFET-based NOT gate using a compact semi-empirical model, already proposed by us.

We started our analysis by evaluating noise margin and static power in different voltage supply and temperature conditions. We observed very similar results with some slight differences. In particular the noise margin decreases and static power increases with temperature, so it can be asserted that low temperature is the most advantageous condition. This is true except for the case 100 K - 200 mV where noise margin is much lower than the expected value due to the double peak in gain function. In terms of power, it should be also noted that decreasing temperature from 200 K to 100 K does not produce any remarkable result.

Moreover we have also applied the proposed procedure to analyze the effects of temperature in the design of analog circuits based on CNTFET [13].

Currently we are studying the effects of temperature [20] and of noise [21-25] in other circuits based on CNTFETs and we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [26-27].

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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