

# Comparative Analysis of Noise in Current Mirror Circuits based on CNTFET and MOS Devices

Roberto Marani<sup>1</sup> and Anna Gina Perri<sup>2,\*</sup>

<sup>1</sup>Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy

<sup>2</sup>Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, Italy

(\*) Corresponding author: annagina.perri@poliba.it  
(Received: 23 March 2021 and Accepted: 24 April 2021)

## Abstract

*In this paper we study an application of CNTFET in the design of current mirrors, key components of analogue circuits, in order to examine the noise behavior of CNTFETs. We compare the CNTFET with a MOSFET of comparable scale and we present the results obtained using simulation for two different current mirror circuits, each time with different current values. To achieve this goal we use a semi-empirical compact CNTFET model, already proposed by us, including noise source contributions, and the BSIM4 model for MOS device. After the simulation of the I-V curves, the differential output resistance and the output impedance at various frequencies, we present the spectral density of output noise current, obtaining for all proposed cases that the output noise current is always higher for the CNTFET than for the MOS device.*

**Keywords:** CNTFET, MOSFET, Modelling, Circuit mirror circuits, Static and dynamic analysis, Noise behaviour.

## 1. INTRODUCTION

One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [1].

As it is known, the carbon nanotubes consist of a hexagonal mesh of carbon atoms wrapped in cylinder shapes. Depending on the chirality, electronic band structure of CNT changes, band gap may appear making them semiconductors, or may not appear, making them conductors.

For conventional CNTFET, also denoted as C-CNTFET, we already proposed a compact, semi-empirical model [2].

Then we introduced some improvements [3] to allow an easy implementation both in SPICE, using ABM library, and in

Verilog-A, and our model has been implemented to carry out analysis of CNTFET-based A/D circuits [4-8].

In this paper we present a simulation study of the application of CNTFET for high frequency current mirrors using two types of circuits: the cascode current mirror and the self-biased current mirror, starting from the design of the basic current mirror already proposed by us in [9].

At first we compare the proposed circuits with the same based on MOSFET device, showing the output I-V characteristics, the output differential conductances at various output voltages, the output admittance at various frequencies.

Then we analyze and discuss the spectral density of output noise current, comparing the two considered technology, highlighting that the output noise for CNTFET

is no more than three times higher (10 dB) than for the MOS, but at some frequency and current we foresee no more than two (6 dB) times higher.

The presentation is organized as follows. A brief review of CNTFET and MOSFET models used is presented in Section 2, together with the analysis of the main noise sources and relative equivalent circuit.

The design of the two current mirrors proposed is described in Sections 3 and 4, together with the discussion of simulation results.

The conclusions and future developments are described in Section 5.

## 2. A BRIEF REVIEW OF CNTFET AND MOSFET MODELS

### 2.1. I-V Model

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them. In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [10], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h} \sum_p \left[ \ln(1 + \exp \xi_{Sp}) - \ln(1 + \exp \xi_{Dp}) \right] \quad (1)$$

where  $q$  is the electron charge,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature,  $h$  is the Planck constant,  $p$  is the number of sub-bands, while  $\xi_{Sp}$  and  $\xi_{Dp}$ , depending on temperature through the sub-bands energy gap, and the surface potential,  $V_{CNT}$ , have the expressions reported in [2-3].

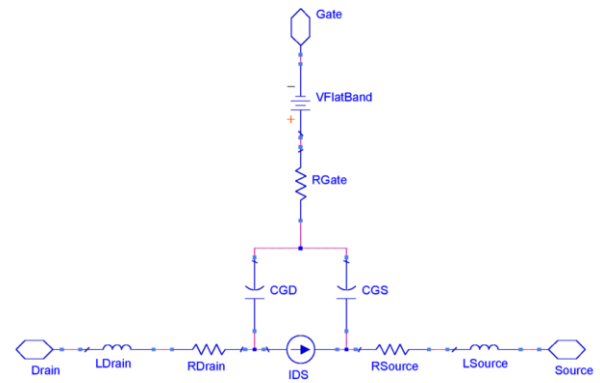
### 2.2. C-V Model

An exhaustive description of our C-V model is widely described in our Refs [7-8] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances  $C_{GD}$  and  $C_{GS}$  are explained:

$$\begin{cases} C_{GD} = q \sum_p \frac{\partial n_{Dp}}{\partial V_{GS}} = q \sum_p \frac{\partial n_{Dp}}{\partial \xi_{Dp}} \frac{\partial \xi_{Dp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q \sum_p \frac{\partial n_{Sp}}{\partial V_{GS}} = q \sum_p \frac{\partial n_{Sp}}{\partial \xi_{Sp}} \frac{\partial \xi_{Sp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behaviour, it is necessary to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

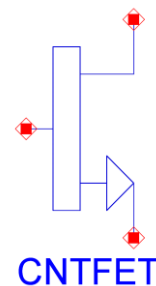
In this paper we have achieved this goal using an empirical method [11], more suitable for simulations in CAD environment, obtaining the equivalent circuit of Figure 1.



**Figure 1.** Equivalent circuit of a n-type CNTFET.

It is similar to a common MOSFET one [12] and is characterized by the flat band generator  $V_{FB}$ , the quantum capacitances  $C_{GS}$  and  $C_{GD}$ , the inductances of the CNT  $L_{Drain}$  and  $L_{Source}$  and the resistors  $R_G$ ,  $R_D$  and  $R_S$ , in which the parasitic effect due to the electrodes are also included.

Figure 2 shows the CNTFET symbol used in the following simulations.



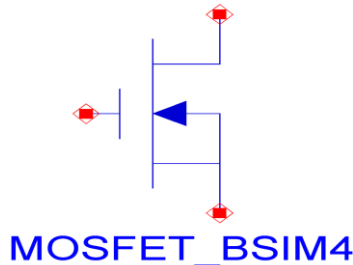
**Figure 2.** CNTFET symbol.

For the MOSFET model we use the BSIM4 model of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [13] and refers to a family of MOSFETs for integrated circuit design.

In this work BSIM4 has been used for the 32 nm technology nodes. The MOSFET parameters for BSIM4 model were obtained by Predictive Technology Model (PTM) web site from the Nanoscale Integration and Modelling Group of Arizona State University. In particular we have selected MOSFET sizes in order to obtain output characteristics comparable to those of CNTFET.

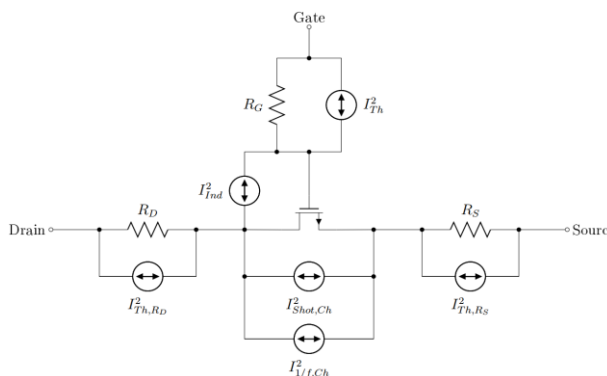
Figure 3 shows the MOSFET symbol, which refers to BSIM4 model.



**Figure 3.** MOSFET symbol.

Regards to noise model, in our Reference [14] we have already proposed a compact noise model of CNTFET and therefore we suggest the reader to consult this paper.

Figure 4 shows the proposed CNTFET noise model, including five different noise sources.



**Figure 4.** The proposed CNTFET noise model, including the main noise sources method [14].

In particular we have considered in [14] the main noise sources, which are:

1. Thermal noise of  $R_G$
2. Thermal noise of  $R_S$  and  $R_D$
3. Channel thermal noise and shot noise
4. Flicker noise
5. Channel-induced gate noise.

The gate resistance  $R_G$ , implemented as a lumped element with a small value ( $\sim 2 \Omega$ ), produces a thermal noise, whose Power Spectral Density (PSD) is:

$$S_{Th,RG} = 4kT/R_G \quad (3)$$

The tube end-regions highly doped show high resistances  $R_S$  and  $R_D$  ( $\sim k\Omega$ ), and their contribution to the power spectral density is in agreement with Eqn. (3).

For the channel thermal and shot noise, conventional noise theory for long-channel devices [15] describes the power spectral density of drain noise as:

$$S_{Th,Ch} = 4kT\gamma g_{d0} \quad (4)$$

being  $g_{d0}$  the channel conductance at  $V_{DS} = 0$  V.

The parameter  $\gamma$  is the so-called *white noise gamma factor*. This index depends on the operating status of the device and classical theory predicts that it is equal to 2/3 when devices operates in saturation regime.

This is not satisfactory for short-channel devices, for which it is necessary to consider a white noise gamma factor in a range between 2 and 3 [16], so we set it to 2.5.

In ballistic devices the main obstacle to carrier flow is not scattering but a potential barrier near the source end of the transistor. The injection of carriers over this barrier follows the Poisson statistics, which results in shot noise [17].

Mechanism as long-range Coulomb interactions and the Pauli exclusion principle can yet introduce correlation between successive injection events [18].

Because of this correlation between noise source, there is a reduction of the noise power spectral density, below the conventional value of  $2qI_{DS}$ .

The resulting suppressed channel shot noise can be expressed as:

$$S_{\text{Shot,Ch}}=2qI_{\text{DS}} \cdot F(I_{\text{DS}}) \quad (5)$$

where  $F(I_{\text{DS}})$ , i.e. depending on  $I_{\text{DS}}$ , is called *Fano factor*.

Its value is between 0 and 1 and the value of  $F$  can be taken from empirical graph in [16].

In this paper the Fano factor used has been obtained by fitting the curves reported in [18].

The description of flicker noise is well explained in [19-20].

According to the empirical law proposed by Hooge [20], we considered the flicker noise in CNTFETs, whose power spectral density is:

$$S_{1/f,\text{Ch}}=A_{\text{H}} \left( \frac{I_{\text{DS}}^2}{f} \right) = \left( \frac{\alpha_{\text{H}}}{n} \right) \left( \frac{I_{\text{DS}}^2}{f} \right) \quad (6)$$

It is possible to notice that the flicker noise is scaled by the noise amplitude  $A_{\text{H}}$ , which is the ratio of the material-dependent Hooge constant  $\alpha_{\text{H}}$  and the number of carriers  $n$  in the channel.

In this paper we have chosen the value of  $\alpha_{\text{H}}$  equal to  $10^{-4}$ , that is a standard number for un-optimized semiconductor [20].

Another type of intrinsic noise that should be considered in CNTFETs is the *channel-induced gate noise*. Van der Ziel has shown that its power spectral density can be described as [15]:

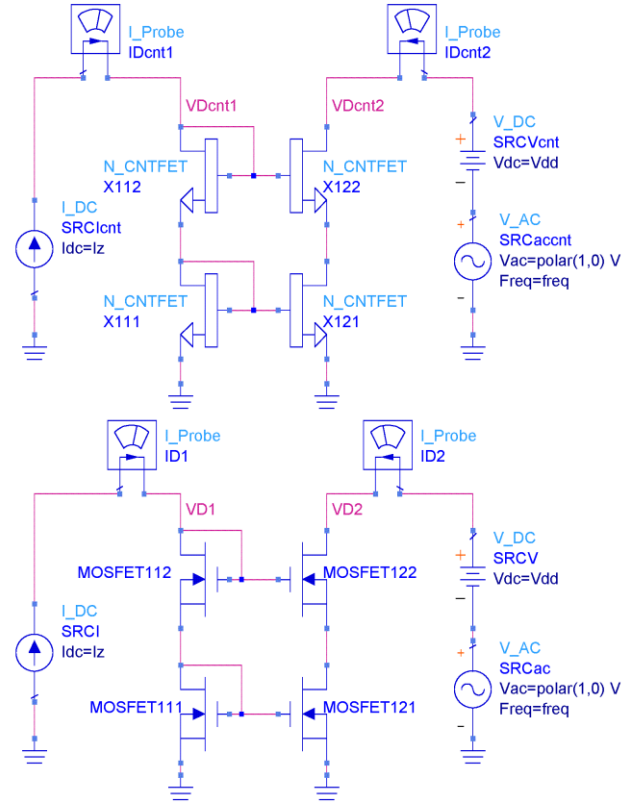
$$S_{\text{ind}}=4kT\delta \left( \frac{\omega^2 C_{\text{GS}}^2}{5g_{\text{d0}}} \right) \quad (7)$$

Due to the lack of theoretical treatment of this type of noise, for ballistic devices we assumed  $\delta$  equal to  $4/3$ , considering for correlation between noise sources the value 0.395j [16].

Moreover in this paper we have not considered the noise sources due to CNT-metal contact Schottky barrier, because our model has been structured for CNTFETs which have no Schottky contacts.

### 3. CASCODE CURRENT MIRROR

The cascode current mirror is a two stage current mirror and consists in four active component as shown in Figure 5.



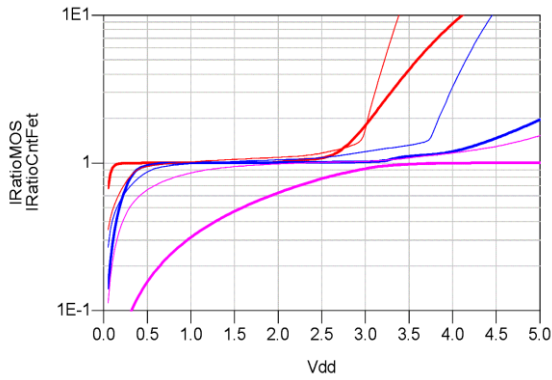
**Figure 5.** Cascode current mirror: on top the CNTFET version, on bottom the MOS version.

We put the current source on the left side, input, and voltage generators on the right side, which is the output. We will discuss briefly this circuit to pay more attention to the self-biased circuit.

We present the ratio of the output current to the input current in Figure 6, where the obtained results for CNTFET and MOS circuit are considered for three input currents, 1 uA (in red), 10 uA (in blue) and 100 uA (in violet).

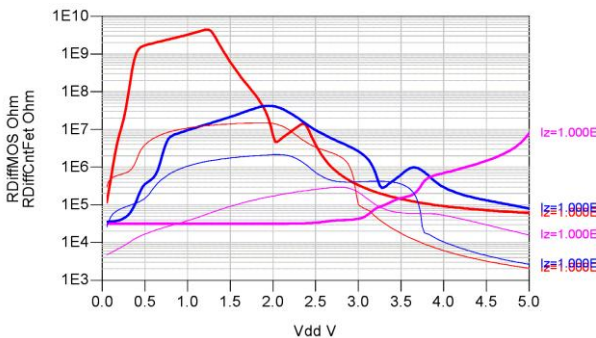
Except for 100  $\mu\text{A}$  current, the CNTFET circuit presents curves that are more near 1 for a larger interval of output voltage than the curves of the MOS circuit.

For 100  $\mu\text{A}$  current the MOS circuit has a quite good curve, while the CNTFET circuit works correctly only over 3 V output voltage.



**Figure 6.** Ratio of the output current divided to the input current. For the CNTFET circuit the curves are bold lines, while for the MOS circuit the curves are thin lines.

In Figure 7 we present the output resistance, the values for the CNTFET circuit are almost always higher the values of the MOS circuit.



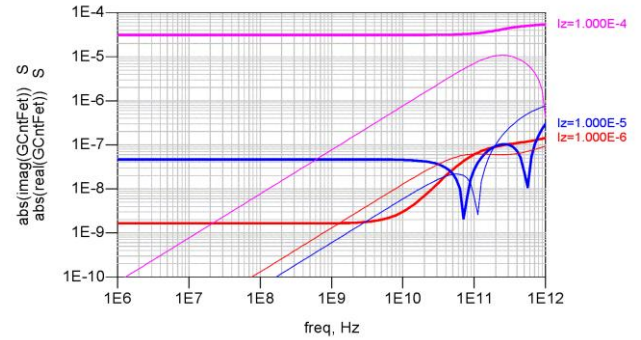
**Figure 7.** Ratio of the output current divided to the input current. Curves as in Figure 6.

The simulation result for small signal in linear approximation allows us to show the output admittance in Figures. 8 and 9. The output voltage is held constant at 1 V for all currents.

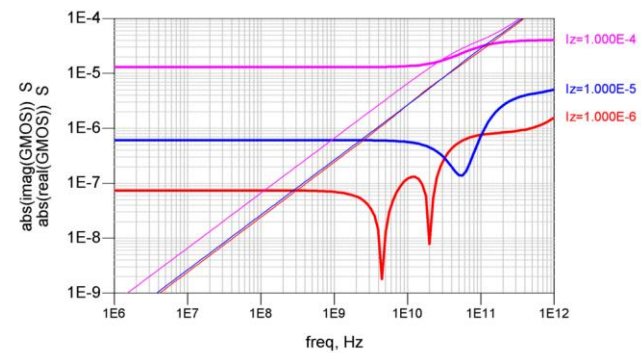
The graphs show that the output could be expressed, at lower frequency, as a parallel of a resistor, a capacitor and the output current source.

The spectral density of noise current is reported in Fig. 10.

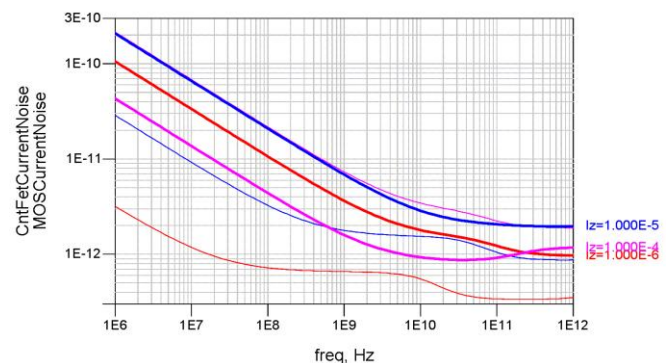
We see that the CNTFET circuit has an higher noise than the MOS, but over 1 GHz it is no more than four times larger.



**Figure 8.** Differential output admittance for the CNTFET circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.



**Figure 9.** Differential output admittance for the MOS circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.

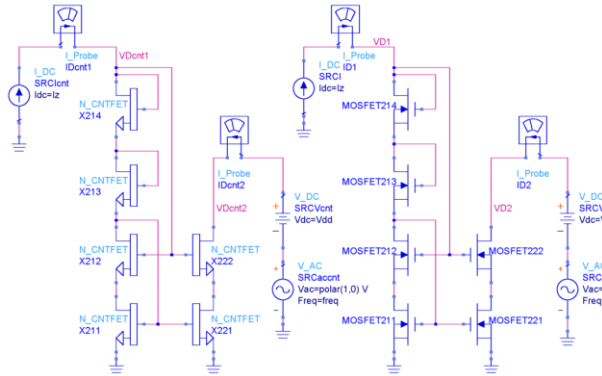


**Figure 10.** Spectral density of the output noise current for the CNTFET and for the MOS circuit, values in  $A Hz^{-1/2}$ . Lines as in Figure 6.

The case 100  $\mu A$  current is not interesting since chosen the output voltage for these noise simulation does not allows a good behavior for the CNTFET current mirror circuit.

#### 4. SELF-BIASED CURRENT MIRROR

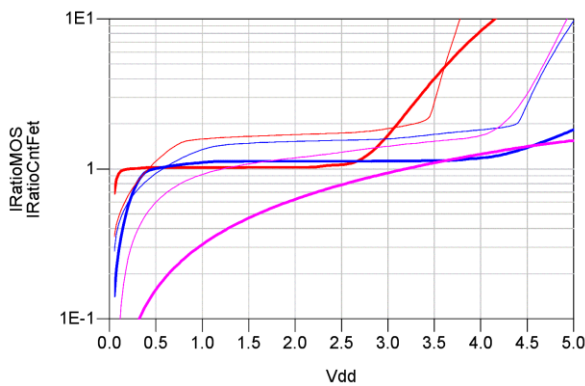
The self-biased current mirror is a more complex circuit and consists in six active component as shown in Figure 11.



**Figure 11.** Self-biased current mirror: on left the CNTFET version, on right the MOS version.

Again, for both circuits, we placed the reference current source on the left side, the input, while on the right side, the output, we placed the voltage sources.

From the static simulation, Figure 12 presents the ratio of the output current to the input current.

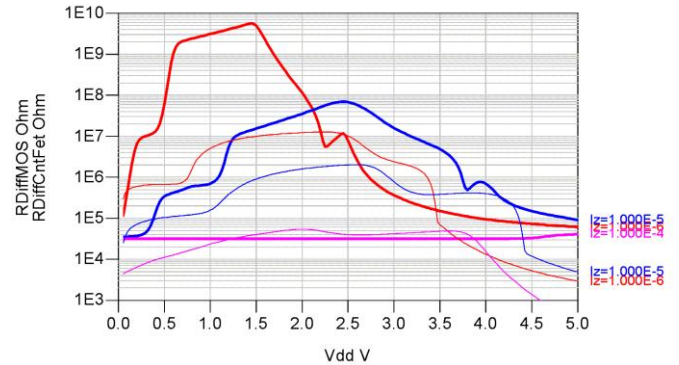


**Figure 12.** Ratio of the output current divided to the input current. Lines as in Fig. 6.

At 1  $\mu\text{A}$  and at 10  $\mu\text{A}$  current the CNTFET circuit has values more near to 1 and more stable than the MOS circuit values, but for 100  $\mu\text{A}$  the curve of the CNTFET circuit is not good at all.

In Figure 13 we plot the differential output resistance of the circuit, in the case of the CNTFET circuit the values are

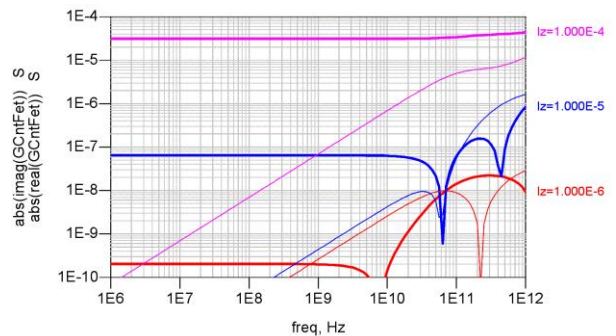
higher in almost all cases than the values for MOS circuit.



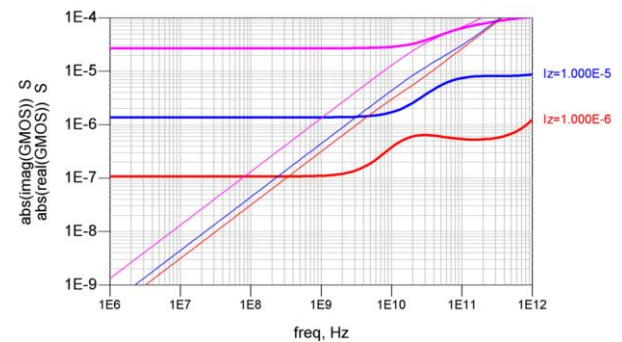
**Figure 13.** Differential output impedance of the current mirror circuits. Lines as in Fig. 6.

The curves of the output admittance are shown in Figures 14 and 15. The output voltage is held constant at 1.5 V for all currents.

These graphs have a behavior similar of those seen for the previous circuit.

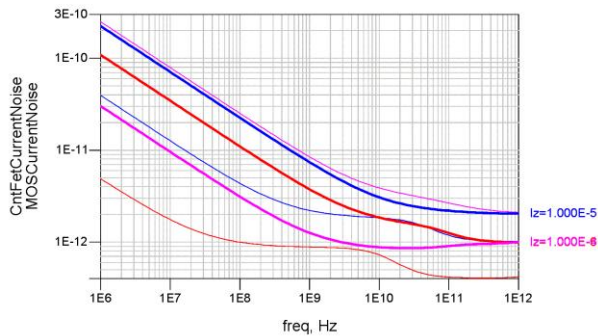


**Figure 14.** Differential output admittance for the CNTFET circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.



**Figure 15.** Differential output admittance for the MOS circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.

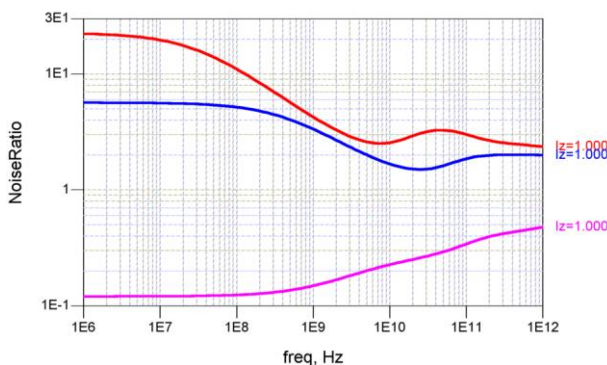
Fig. 16 shows the spectral density of the output noise current.



**Figure 16.** Spectral density of the output noise current for the CNTFET and for the MOS circuit, values in  $A Hz^{-1/2}$ .

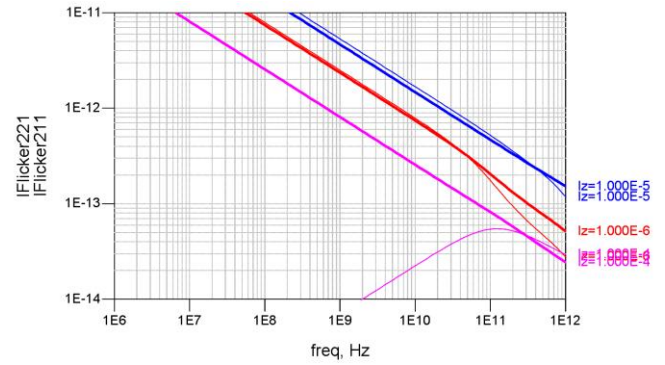
Again we can see higher noise in the CNTFET circuit all cases, but over 1 GHz it is just a bit more three times higher for a smaller interval of frequencies at 50 GHz, otherwise between one and three time larger as shown in Figure 17.

Only for the case of the CNTFET circuit, we present in Figure 18, Figure 19 and Figure 20 respectively the spectral density of noise current for the component coming from the flicker, the shot and the thermal coming from two devices X211 and X221 (see Fig. 11).

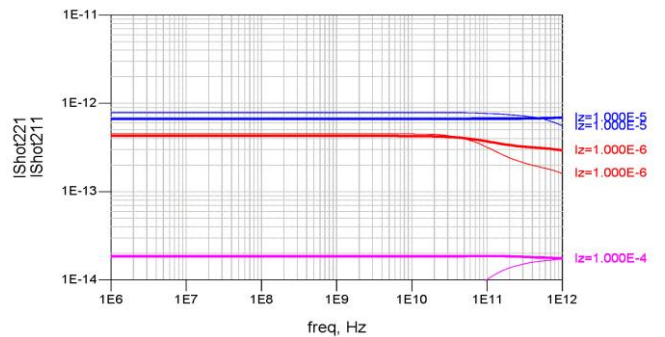


**Figure 17.** Ratio of the noise current spectral density of the CNTFET circuit divided by the noise current spectral density for the MOS circuit. Lines as in Fig. 6.

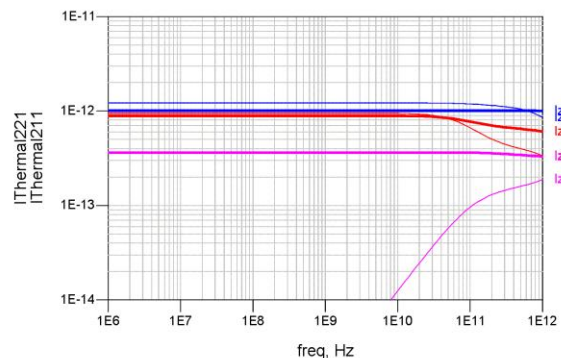
Except the case of the 100  $\mu A$  current, devices contribute evenly to the output noise except at higher frequencies.



**Figure 18.** Spectral density of the output noise current for the CNTFET, values in  $A Hz^{-1/2}$  (Flicker component). The thick lines are for the X221 device, the thin lines for the X211 device (see Fig. 11).



**Figure 19.** Spectral density of the output noise current for the CNTFET, values in  $A Hz^{-1/2}$  (Shot component). The thick lines are for the X221 device, the thin lines for the X211 device (see Fig. 11).



**Figure 20.** Spectral density of the output noise current for the CNTFET, values in  $A Hz^{-1/2}$  (Thermal component).

## 5. CONCLUSIONS AND FUTURE DEVELOPMENTS

We have presented a simulation study of two current mirrors based on CNTFET: cascode current mirror and self-biased current mirror.

We compared the examined circuits with the same circuits using MOS device, showing the output I-V curves, the output differential conductances at various output voltages, the output admittance at various frequencies and the spectral density of output noise current.

For reference current of 1  $\mu\text{A}$  and 10  $\mu\text{A}$  the output static and dynamic characteristics are better in the case of CNTFET, but for all cases the output noise current is always higher for the CNTFET than for the MOS.

The output noise for CNTFET is no more than three times higher (10 dB) than for the MOS, but at some frequency and current we foresee no more than two (6 dB) times higher.

We stress that this estimate depends on the value of Hooge parameter, such as  $\alpha_H$ , depending heavily on the technological process, and whose value must be

determined experimentally.

Similar problems of experimental confirmation are needed for the white noise factor  $\gamma$  and the Fano functions.

Currently we are further working to study the effect of temperature [21-22] and of noise in other circuits based on CNTFETs. Moreover we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [23] and the impact of technology on CNTFET-based circuits performance [24].

We also intend to repeat the proposed simulations using other CNTFET models such the model proposed in literature [25-28] in order to have comparable results.

### CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

### REFERENCES

1. Perri, A. G., Marani, R., “*CNTFET Electronics: Design Principles*”, Editor Progedit, Bari, Italy, (2017).
2. Gelao, G., Marani, R., Diana, R., Perri, A. G., “A Semi-Empirical SPICE Model for n-type Conventional CNTFETs”, *IEEE Transactions on Nanotechnology*, 10 (2011) 506-512.
3. Marani, R., Perri, A. G., “A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software”, *Current Nanoscience*, 7 (2011) 245-253.
4. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., “A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis”, *Current Nanoscience*, 11 (2015) 515-526.
5. Gelao, G., Marani, R., Pizzulli, L., Perri, A. G., “A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part II: Dynamic Analysis”, *Current Nanoscience*, 11 (2015) 770-783.
6. Marani, R., Perri, A. G., “A Simulation Study of Analogue and Logic Circuits with CNTFETs”, *ECS Journal of Solid State Science and Technology*, 5 (2016) M38-M43.
7. Marani, R., Perri, A. G., “Static Simulation of CNTFET-based Digital Circuits”, *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 121-131.
8. Marani, R., Perri, A. G., “Dynamic Simulation of CNTFET-based Digital Circuits”, *International Journal of Nanoscience and Nanotechnology*, 14 (2018) 277-288.
9. Marani, R., Perri, A. G., “Comparison of CNTFET and MOSFET Noise Performance through the Design of Basic Current Mirror”; *International Journal of Research and Reviews in Applied Sciences*, 46(1) (2021) 21-29.
10. S. Datta, S., “*Cambridge Studies in Semiconductor Physics and Microelectronic Engineering 3.*”, New York: Cambridge University Press, (1995).
11. Prégaldiny, F., Lallement, C., Diange, B., Sallese, M., Kammerer, J. B., “*Compact Modeling of Emerging Technologies with VHDL-AMS*. In Huss, S. A. (ed). *Advances in Design and Specification Languages for Embedded Systems*. Dordrecht: Springer Netherlands, (2007).
12. Allen, P. E., Holberg, D. R., “*CMOS Analog Circuit Design*”, Oxford University Press, United Kingdom, (2013).
13. <http://bsim.berkeley.edu/models/bsim4/>, BSIM Group, Berkeley, University of California, USA, (2020).
14. Marani, R., Gelao, G., Perri, A. G., “A Compact Noise Model for C-CNTFETs”, *ECS Journal of Solid State Science and Technology*, 9 (2017) M118-M126.
15. Van der Ziel, A., “*Noise in Solid State Devices and Circuits*”, Ed. Wiley, New York, (1986).
16. Landauer, G. M., Gonzalez, J. L., “A compact noise model for carbon nanotube FETs”, *Proceedings of International Semiconductor Conference Dresden-Grenoble (ISCDG)*, (2012).



17. Navid, R., Jungemann, C., Lee, T. H., Dutton, R. W., “High-frequency noise in nanoscale metal oxide semiconductor field effect transistors”, *Journal of Applied Physics*, 101 (2007) 124501.
18. Betti, A., Fiori, G., Iannaccone, G., “Shot Noise Suppression in Quasi-One-Dimensional Field-Effect Transistors”, *IEEE Transactions on Electron Devices*, 56(9), (2009) 2137-2143.
19. Lin, Y. M., Appenzeller, J., Knoch, J., Chen, Z., Avouris, P., “Low-Frequency Current Fluctuations in Individual Semiconducting Single-Wall Carbon Nanotubes”, *Nano Letters*, 6(5) (2006) 930-936.
20. Hooge, F. H., “1/f Noise Sources”, *IEEE Transactions on Electron Devices*, 41(2) (1994) 1926-1935.
21. Marani, R., Perri, A. G., “A Review on the study of Temperature Effects in the Design of A/D Circuits based on CNTFET”, *Current Nanoscience*, 15 (2019) 471-480.
22. Marani, R., Perri, A. G., “Temperature Dependence of I-V Characteristics in CNTFET Models: A Comparison”, *International Journal of Nanoscience and Nanotechnology*, 17(1) (2021) 33-39.
23. Marani, R., Perri, A. G., “Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits”, *ECS Journal of Solid State Science and Technology*, 9 (2020).
24. Marani, R., Perri, A. G., “Impact of Technology on CNTFET-based Circuits Performance”, *ECS Journal of Solid State Science and Technology*, 9 (2020).
25. Deng, J., Wong, H.-S. P., “A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region”, *IEEE Transactions on Electron Devices*, 54 (2007) 3186-3194.
26. Deng, J., Wong, H.-S. P., “A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking”, *IEEE Transactions on Electron Devices*, 54 (2007) 3195-3205.
27. Lee, C.-S., Pop, E., Franklin, A. D., Haensch, W., Wong, H.-S. P., “A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nmRegime—Part I: Intrinsic Elements”, *IEEE Transactions on Electron Devices*, 62 (2015) 3061-3069.
28. Lee, C.-S., Pop, E., Franklin, A. D., Haensch, W., Wong, H.-S. P., “A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nm Regime—Part II: Extrinsic Elements, Performance Assessment, and Design Optimization”, *IEEE Transactions on Electron Devices*, 62 (2015) 3070-3078.